EE 330
Lecture 6

- Basic Logic Circuits
- Complex Logic Gates
- Pass Transistor Logic

Office Hours

Tuesdays   2:00 p.m.
Thursdays 11:00 a.m.

https://iastate.zoom.us/j/91692566556

Other times by appointment

Send email request and suggest times

Photo courtesy of the director of the National Institute of Health (NIH)

Masks Save Lives

NIH

As a courtesy to fellow classmates, TAs, and the instructor

Wearing of masks during lectures and in the laboratories for this course would be appreciated irrespective of vaccination status

Meeting the real Six-Sigma Challenge
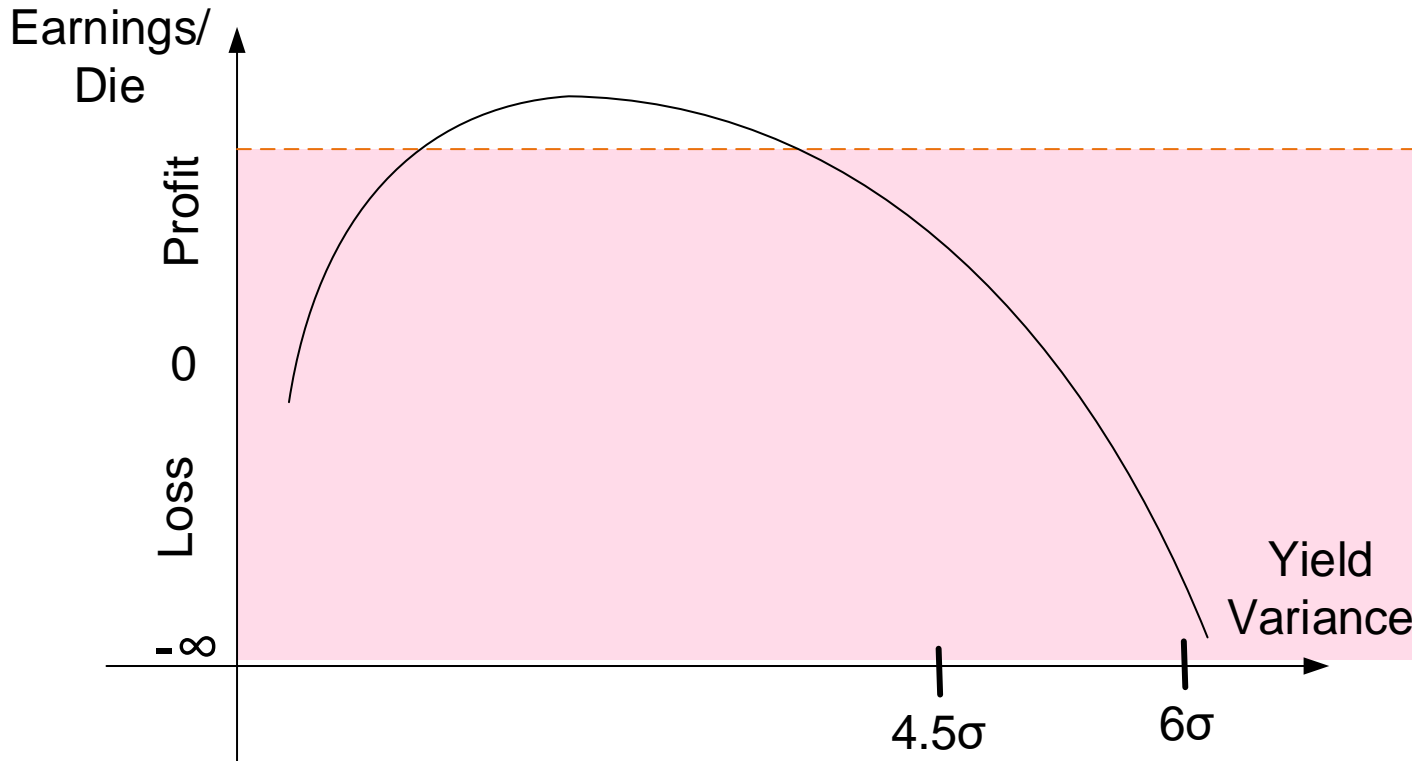
Six-Sigma or Else !!

The concept of improving reliability (really profitability) is good – its just the statistics that are abused!
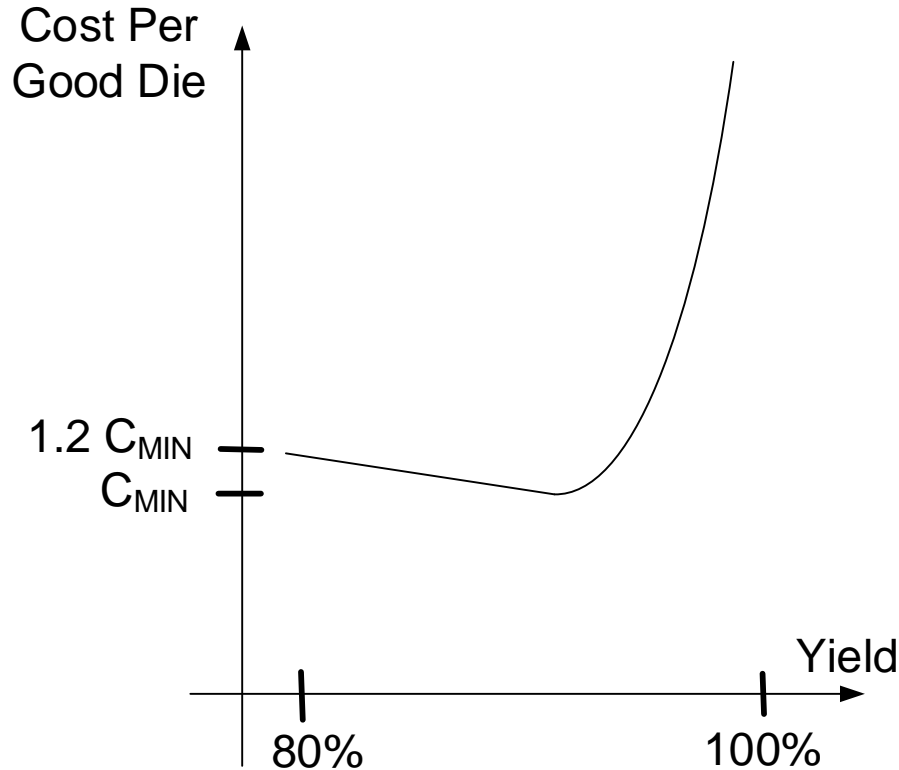
The Reality

Six-Sigma or Else !!

- **Designing for 4.5σ or 6σ yield variance will almost always guarantee large los**

- **Yield targets should be established to optimize earnings not yield variance**
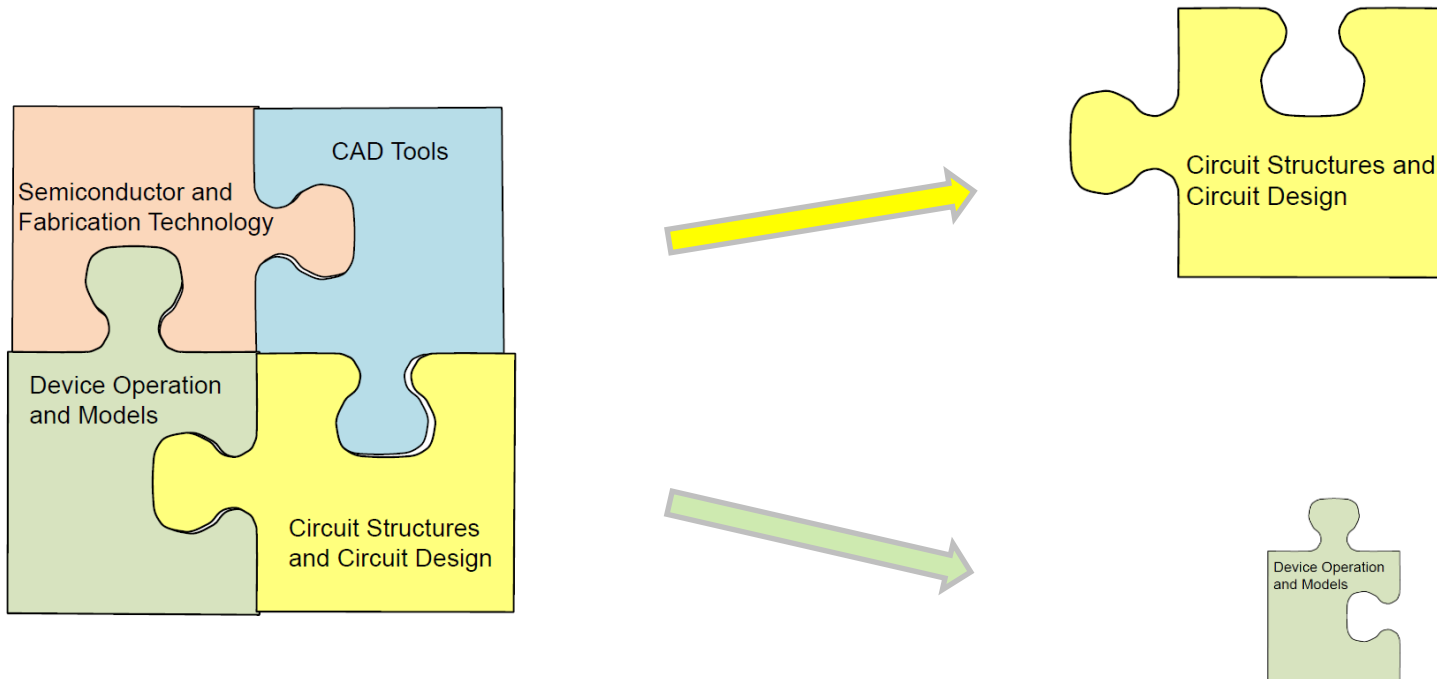
The Reality about Yield

- **Return on improving yield when yield is above 95% is small**
- **Inflection point could be at 99% or higher for some designs but below 50% for others**
- **Cost/good die will ultimately go to ∞ as yield approaches 100%**

Designers goal should be to optimize profit, not arbitrary yield target

Basic Logic Circuits

Basic Logic Circuits

- Will present a brief description of logic circuits based upon simple models and qualitative description of processes

- Will later discuss process technology needed to develop better models

- Will even later provide more in-depth discussion of logic circuits based upon better device models

Models of Devices

- Several models of the electronic devices will be introduced throughout the course
  - Complexity
  - Accuracy
  - Insight
  - Application
- Will use the simplest model that can provide acceptable results for any given application

MOS Transistor
Qualitative Discussion of n-channel Operation

Cross-Sectional View

Bulk

Source

Gate

Drain

n-channel MOSFET

Top View

Source

Drain

Gate
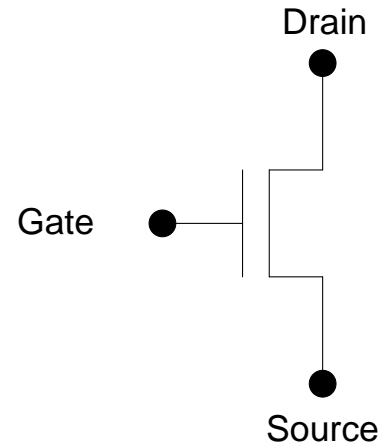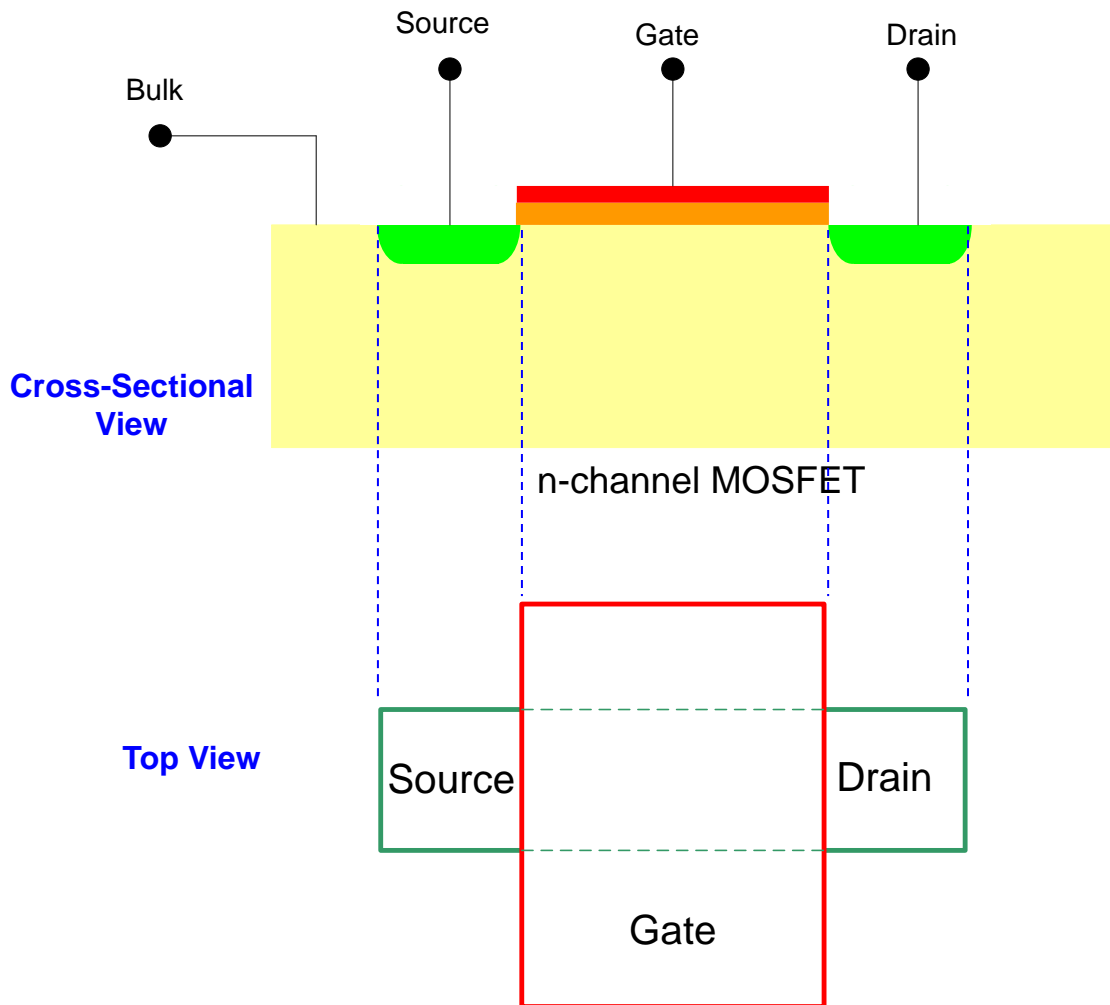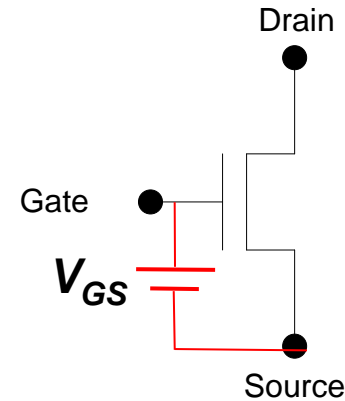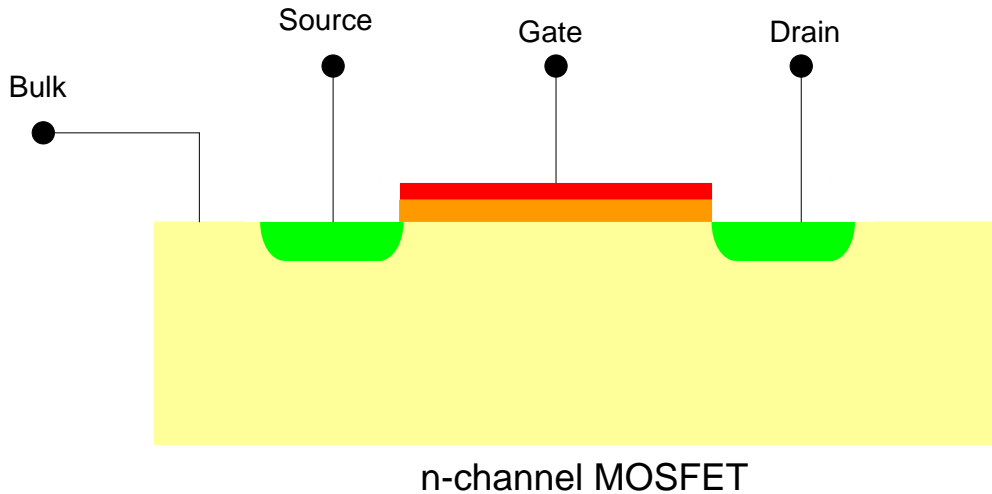
Symbol for n-channel MOSFET

Drain

Gate

Source

n-type

n+-type

p-type

p+-type

SiO$_2$ (insulator)

POLY (conductor)

Designer always works with top view

Complete Symmetry in construction between Drain and Source

MOS Transistor
## Qualitative Discussion of n-channel Operation

n-channel MOSFET

Behavioral Description of Operation of n-channel MOS Transistors Created for use in Basic Digital Circuits

If V_{GS} is large, short circuit exists between drain and source

If V_{GS} is small (or negative), open circuit exists between drain and source

Boolean/Continuous Notation:

V_{DD}

G=1

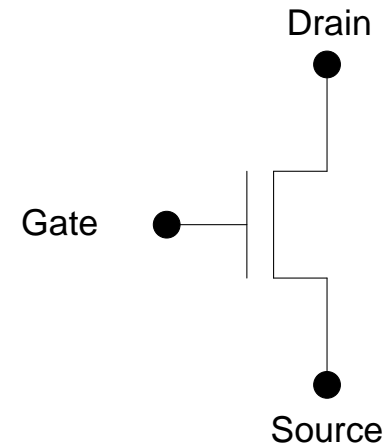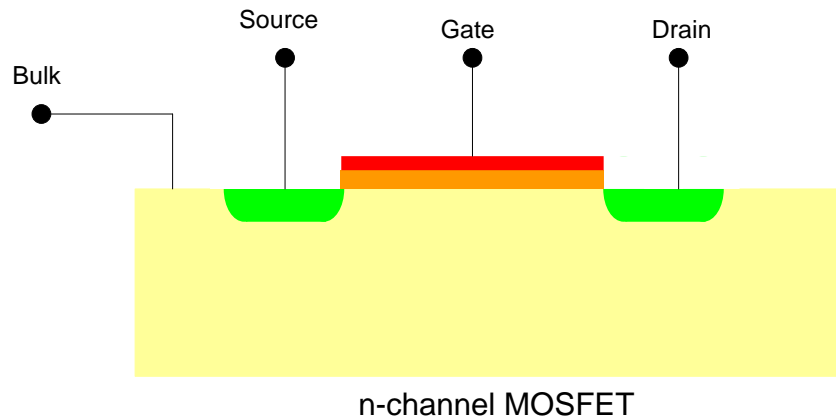**Voltage Axis**

Boolean Axis

0V

G=0
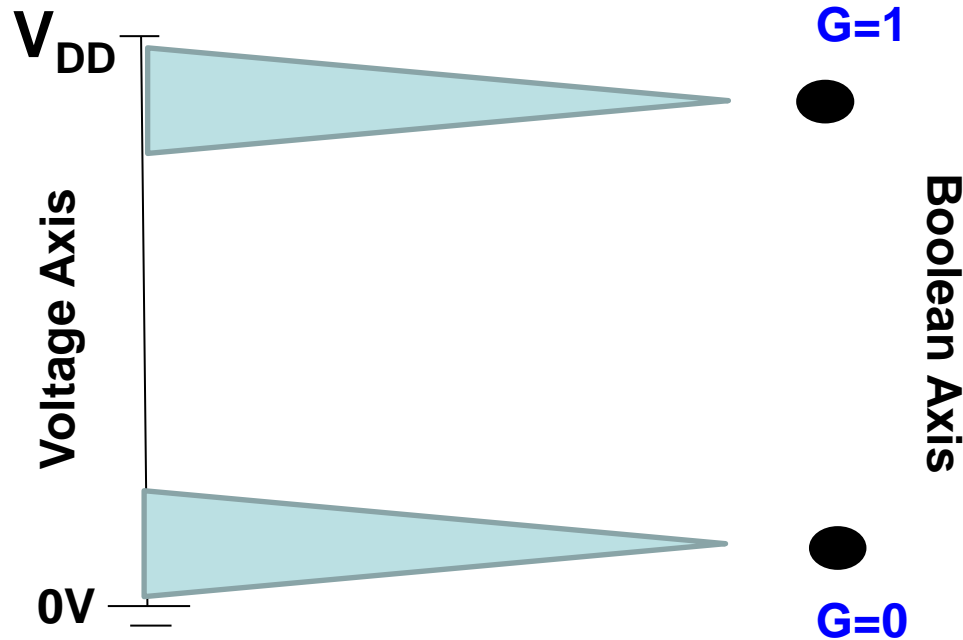
- Voltage Axis is Continuous between 0V and V_{DD}
- Boolean axis is discrete with only two points

Most logic circuits characterized by the relationship between the Boolean input/output variables though these correspond to voltage intervals on the continuous voltage axis

MOS Transistor
Qualitative Discussion of n-channel Operation

Source Gate Drain

Bulk

Drain

Gate

Source

n-channel MOSFET

Equivalent Circuit for n-channel MOSFET
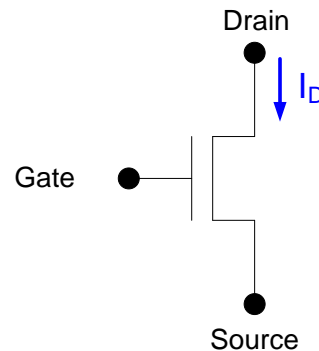
D

D

G = 0

G = 1

S

S
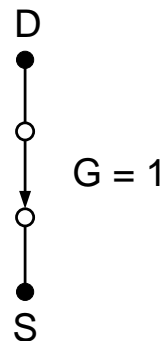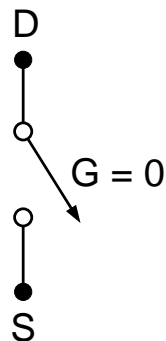
- **Source assumed connected to (or close to) ground**
- $V_{GS}=0$ **denoted as Boolean gate voltage G=0**
- $V_{GS}=V_{DD}$ **denoted as Boolean gate voltage G=1**
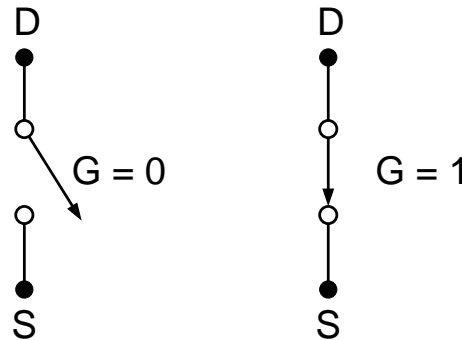- **Boolean G is relative to ground potential**

This is the first model we have for the n-channel MOSFET !

Ideal switch-level model

MOS Transistor MODEL

Drain

I_D

Gate

Source

Equivalent Circuit for n-channel MOSFET **with source as ground**
Termed a Switch-Level Model

D

$G = 0$

S

D

$G = 1$

S

Mathematical model **(not dependent upon Boolean notation):**

$I_D = 0$ if V_{GS} is low (or negative)

$V_{DS} = 0$ if V_{GS} is high
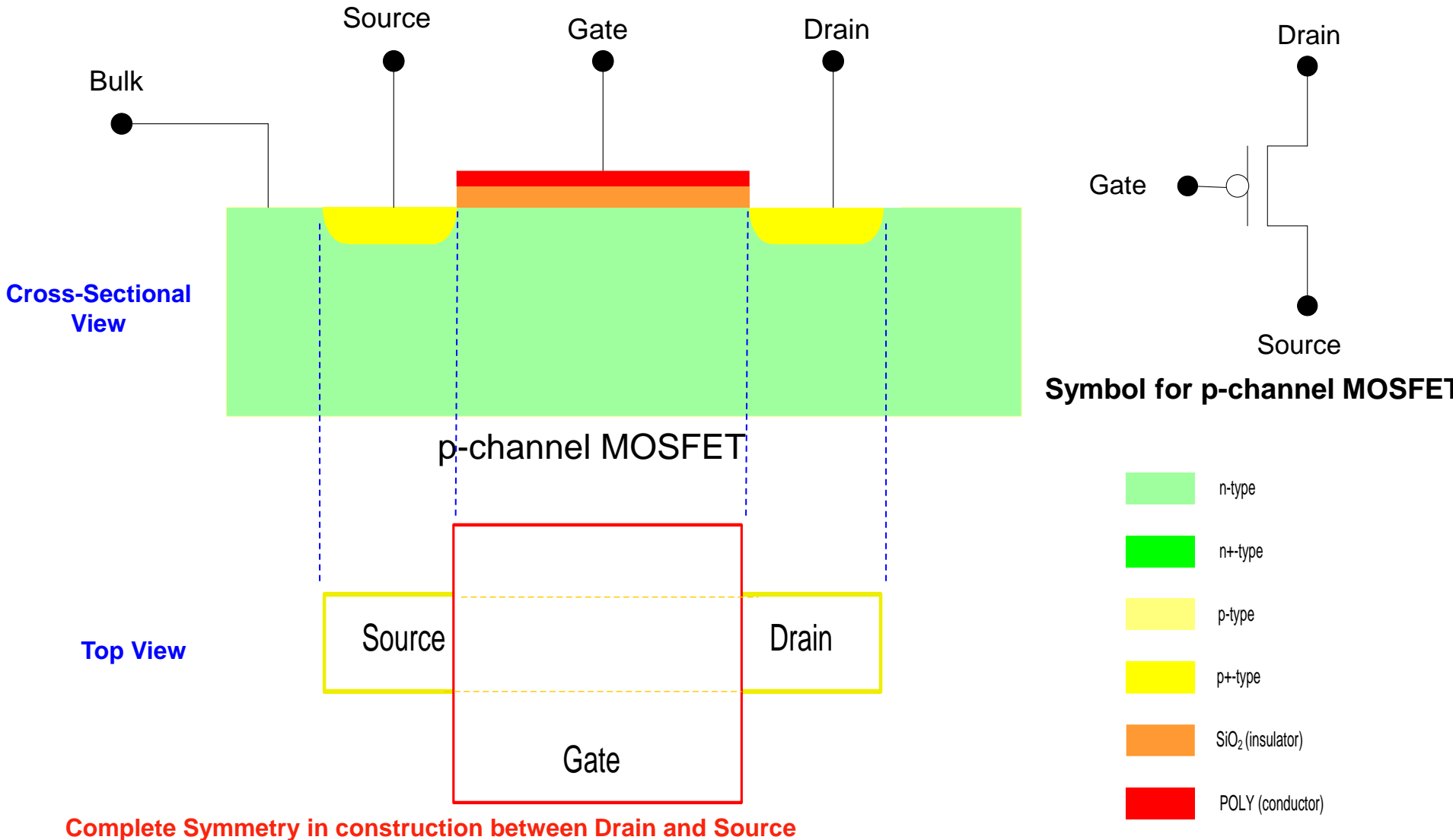
MOS Transistor
Qualitative Discussion of p-channel Operation

Bulk

Source

Gate

Drain

Drain

Gate

Source

Cross-Sectional View

Symbol for p-channel MOSFET

p-channel MOSFET

Top View

Source

Drain

Gate

n-type

n+-type

p-type

p+-type

SiO$_2$ (insulator)

POLY (conductor)

Complete Symmetry in construction between Drain and Source

MOS Transistor
Qualitative Discussion of p-channel Operation

Source Gate Drain
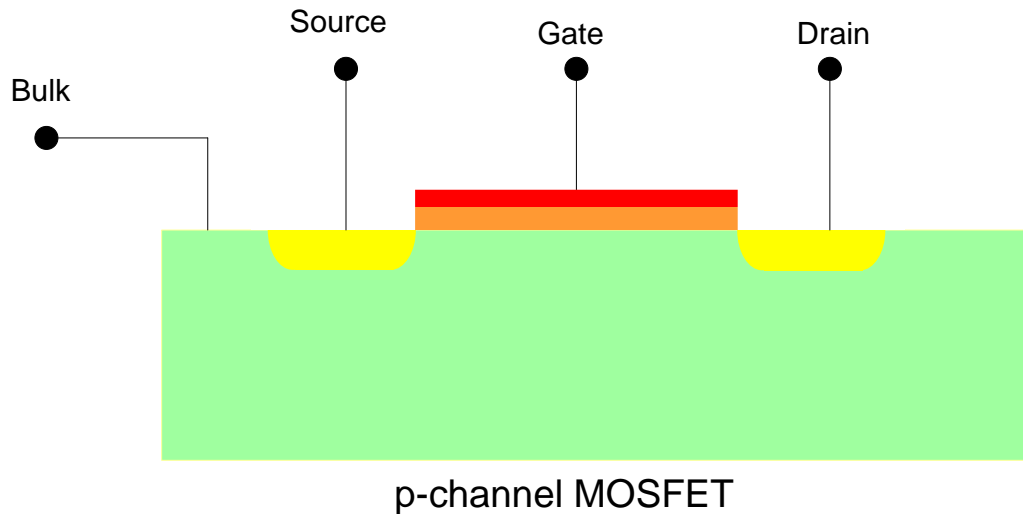
Bulk

Drain

Gate

Source

p-channel MOSFET
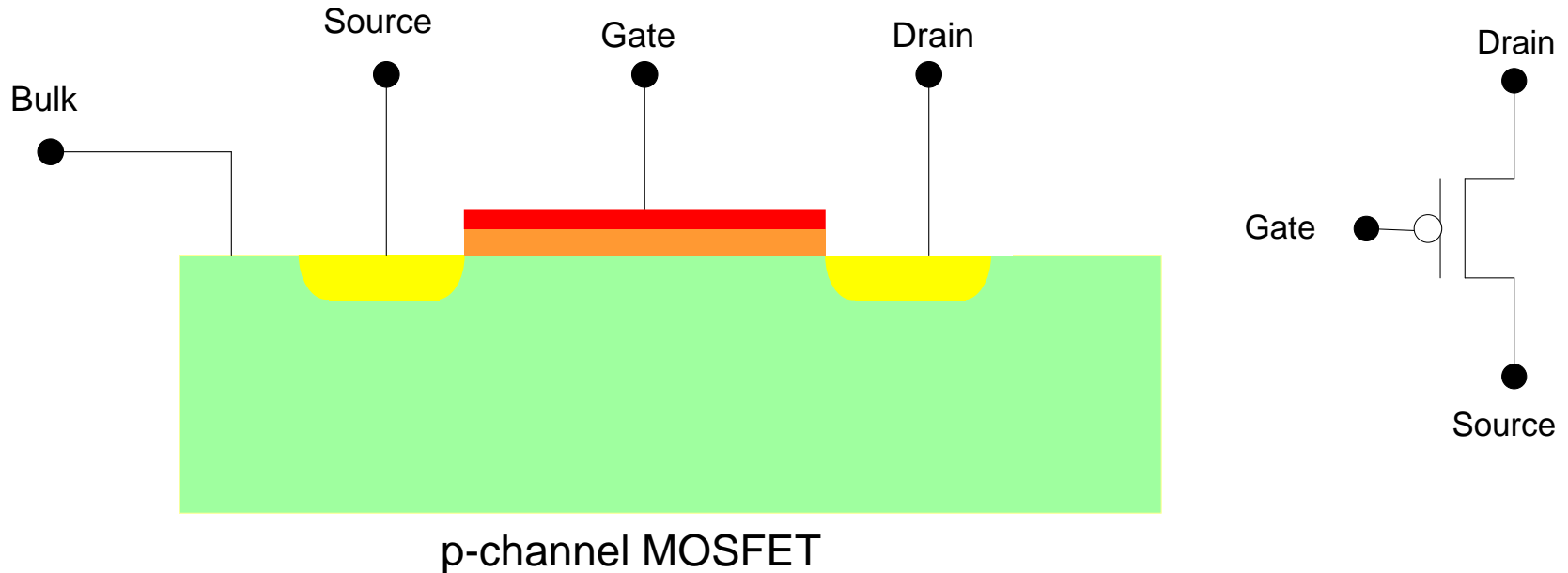
Behavioral Description of Operation of p-channel transistors created for use in basic digital circuits

If V_{GS} is large (and negative), short circuit exists between drain and source
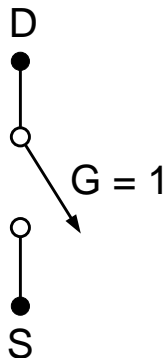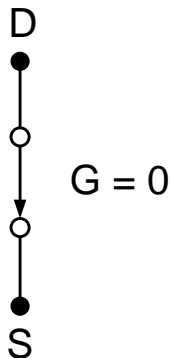
If V_{GS} is small (near 0 or positive), open circuit exists between drain and source

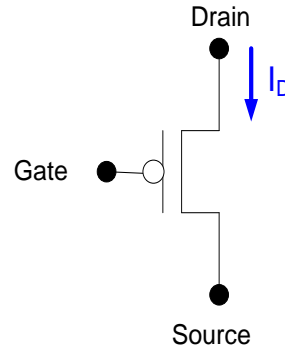# MOS Transistor
Qualitative Discussion of p-channel Operation

Source   Gate   Drain

Bulk

Drain

Gate

Source

p-channel MOSFET

Equivalent Circuit for p-channel MOSFET
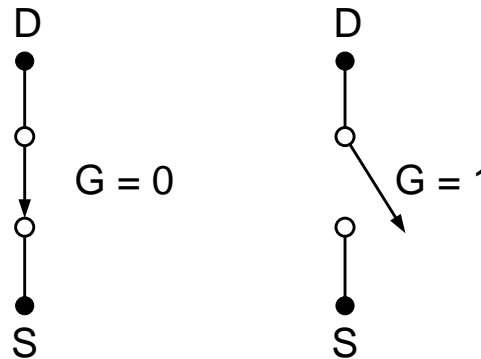
D

D

G = 0

G = 1

S

S
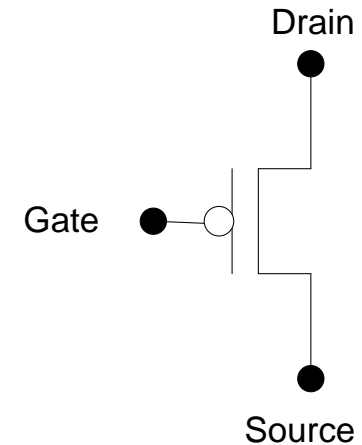
- **Source assumed connected to (or close to) positive V$_{DD}$**
- **V$_{GS}$=0 denoted as Boolean gate voltage G=1**
- **V$_{GS}$= -V$_{DD}$ denoted as Boolean gate voltage G=0**
- **Boolean G is relative to ground potential**

This is the first model we have for the p-channel MOSFET !

MOS Transistor MODEL

Equivalent Circuit for p-channel MOSFET **with Source at VDD**
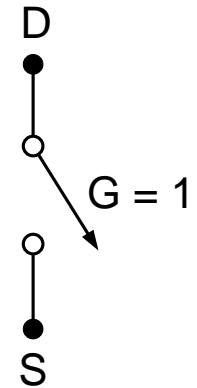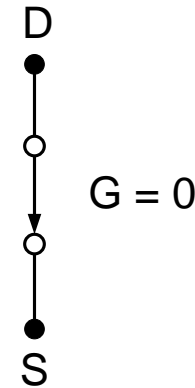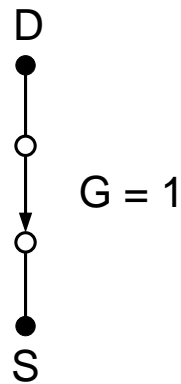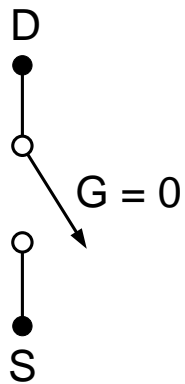
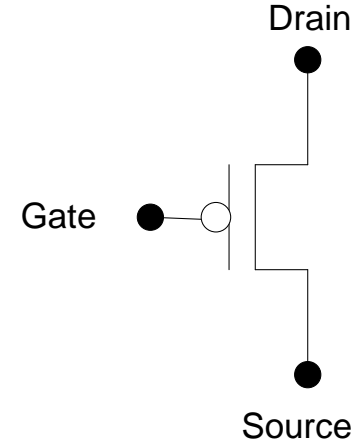**Termed a Switch-Level Model**
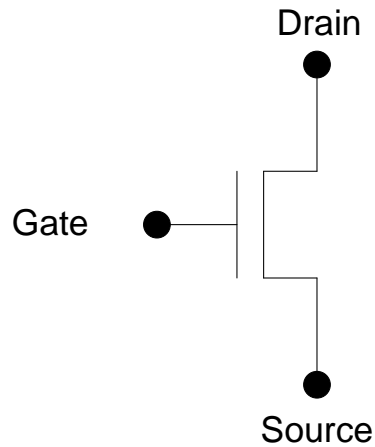

Mathematical model **(not dependent upon Boolean notation):**

$I_D = 0$ if $\left| V_{GSp} \right|$ is small   or V_{GSp} is positive

$V_{DS} = 0$ if $\left| V_{GSp} \right|$ is large   and V_{GSp} is negative

MOS Transistor
Comparison of Operation

Drain

Gate

Source

Drain

Gate

Source

D

D

G = 0

G = 1

S

S

D

D

G = 0

G = 1
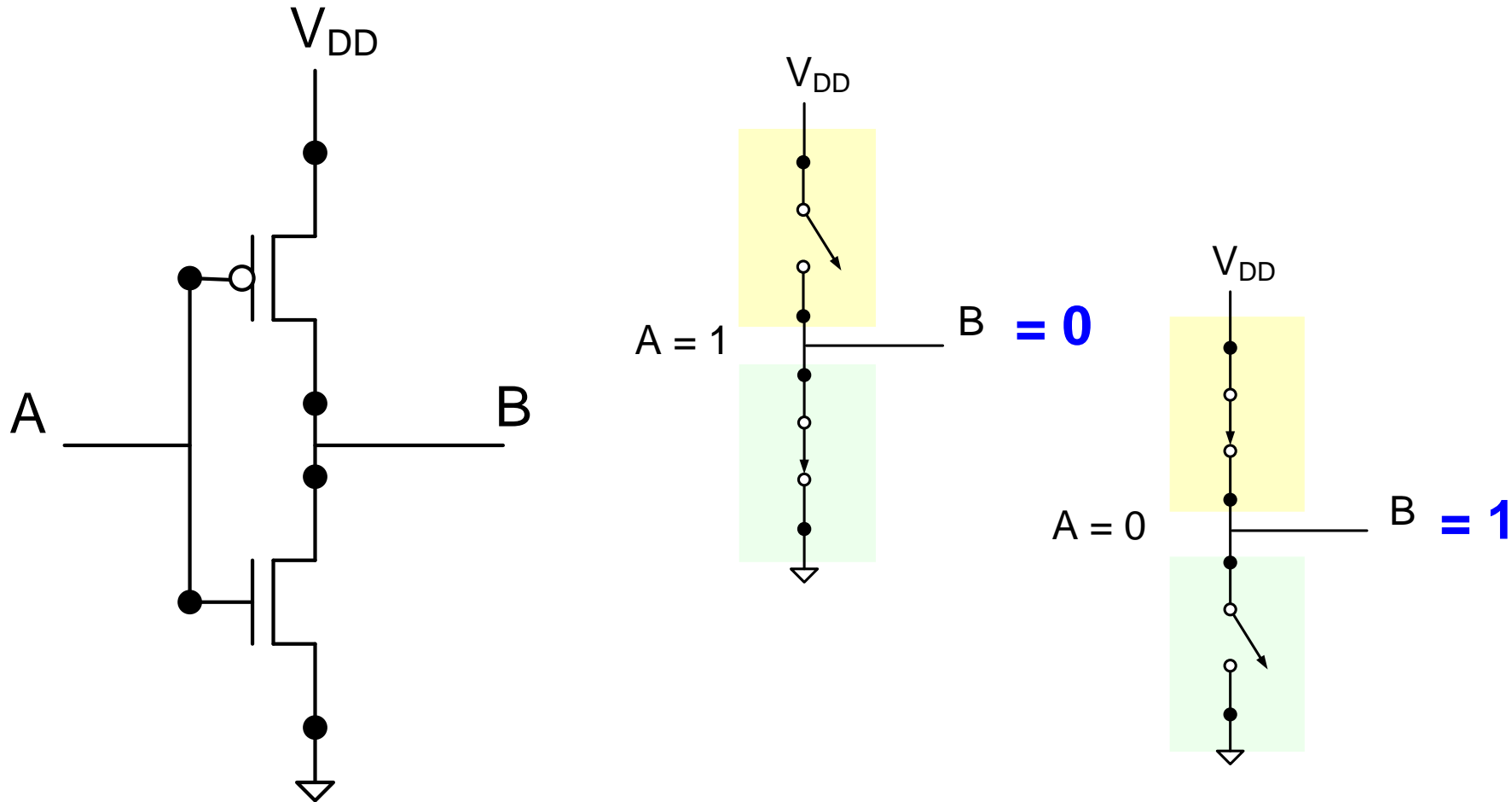
S

S

Source assumed connected to (or close to) ground
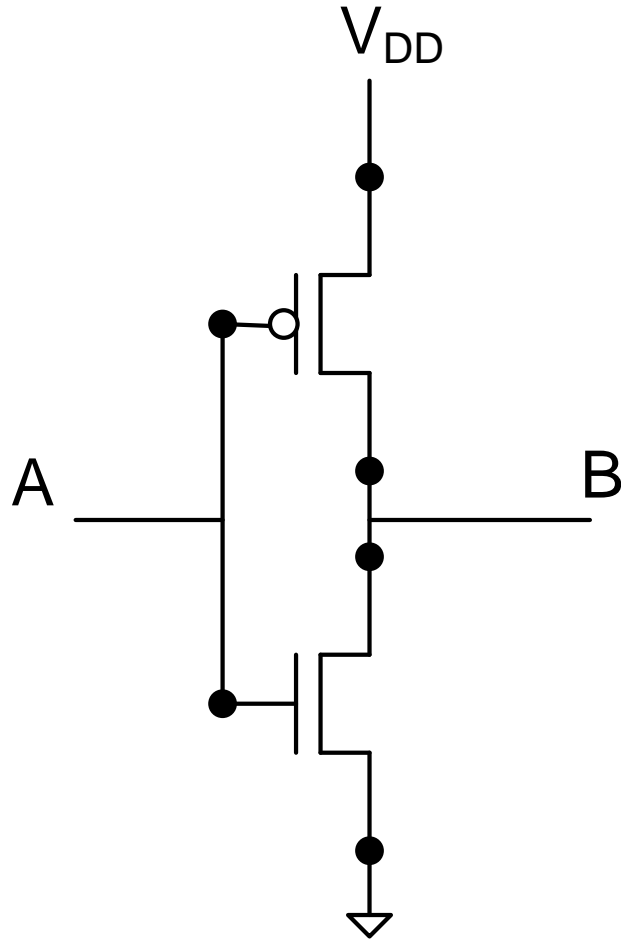
Source assumed connected to (or close to) positive V_{DD} and Boolean G at gate is relative to ground

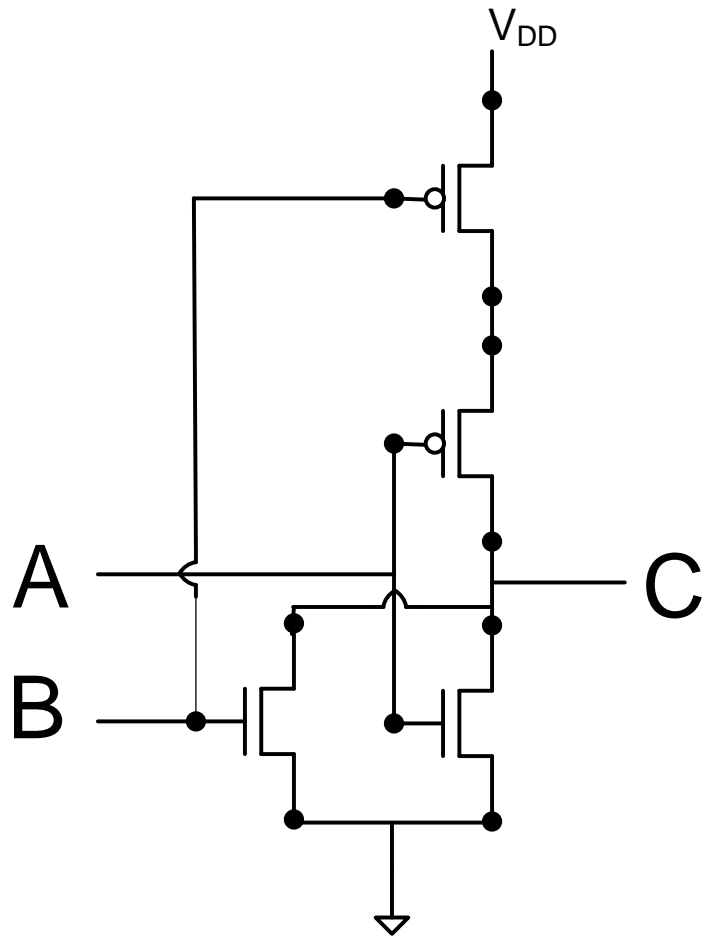# Logic Circuits

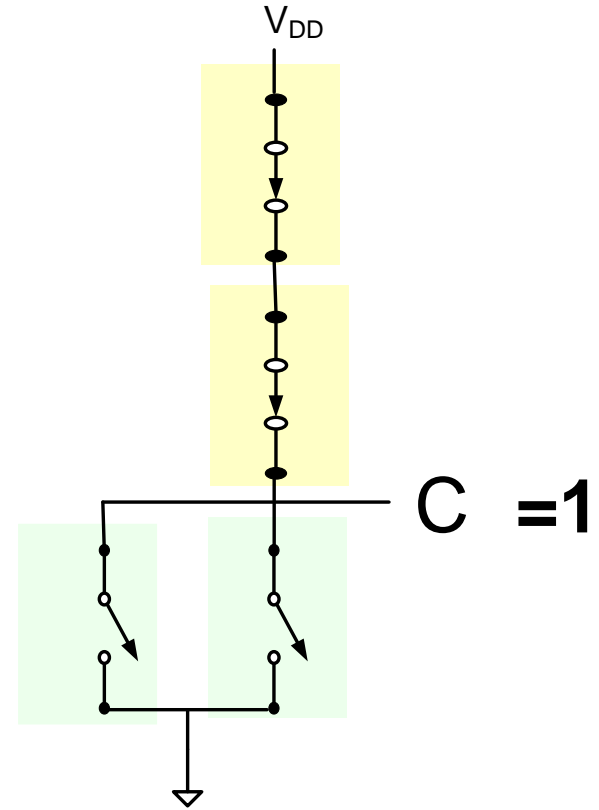
Circuit Behaves as a Boolean Inverter

Logic Circuits

V_{DD}

A

B

Inverter

Truth Table

A	B
0	1
1	0

Logic Circuits

V_{DD}

A

B

C

V_{DD}

A=0

B=0

C **=1**

Logic Circuits

A=1

B=0

C =0

Logic Circuits

V_{DD}

A

B

C

A=0

B=1

V_{DD}

C**=0**
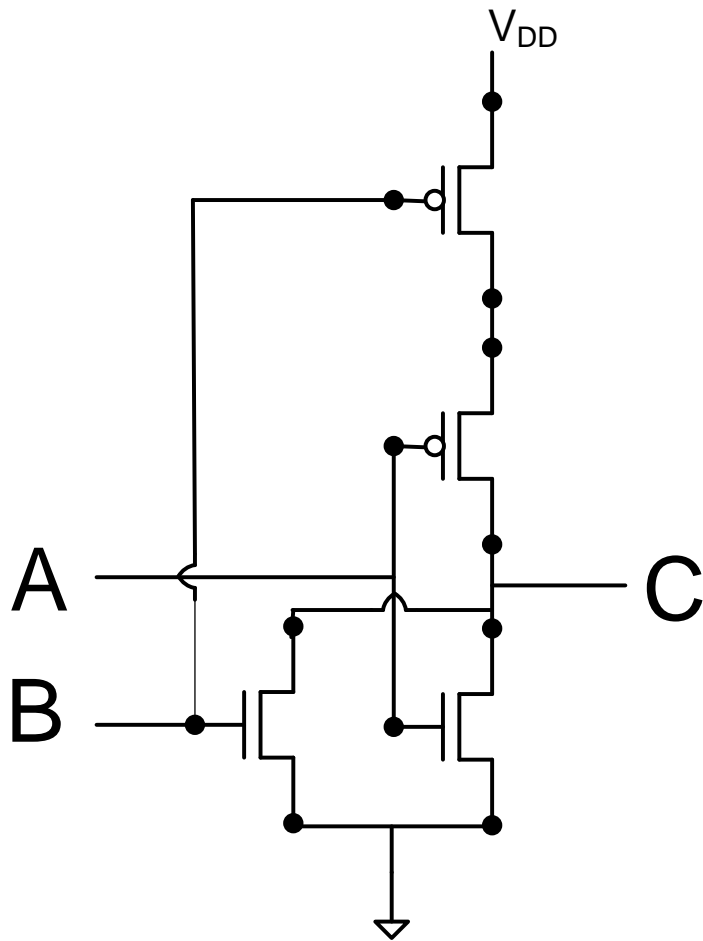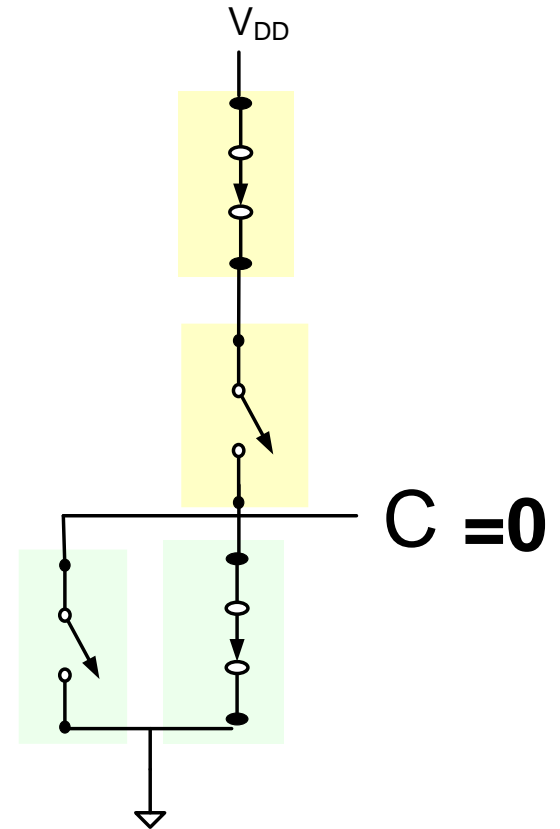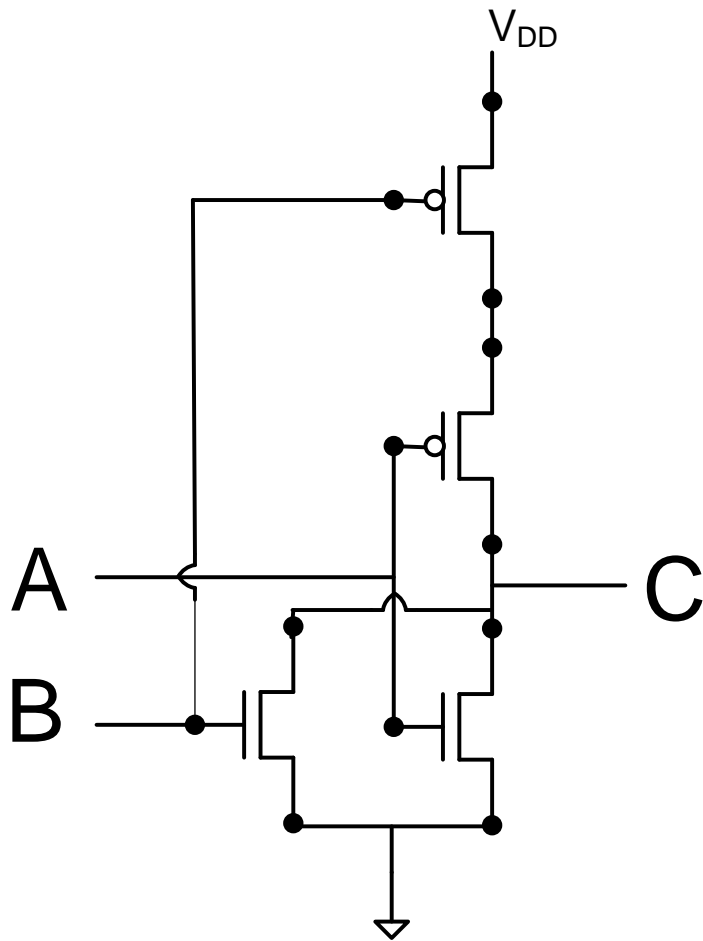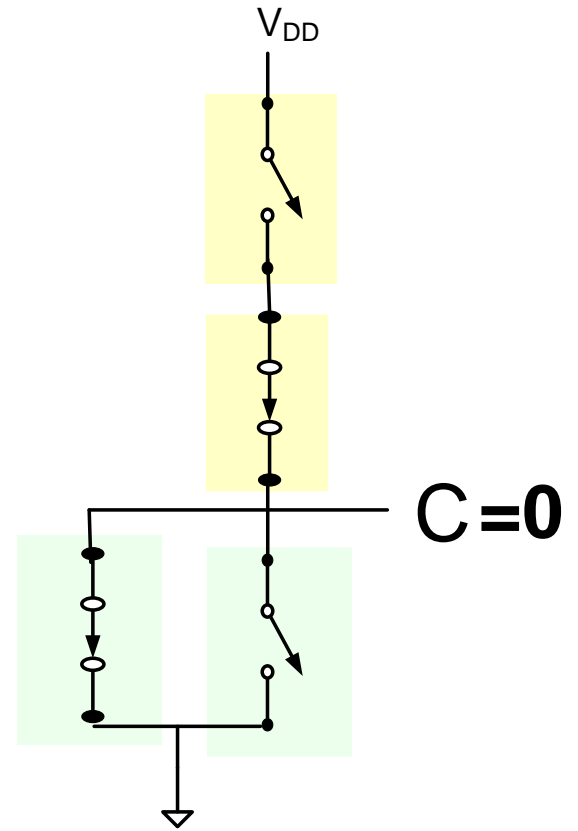
Logic Circuits

A=1

B=1

C =0
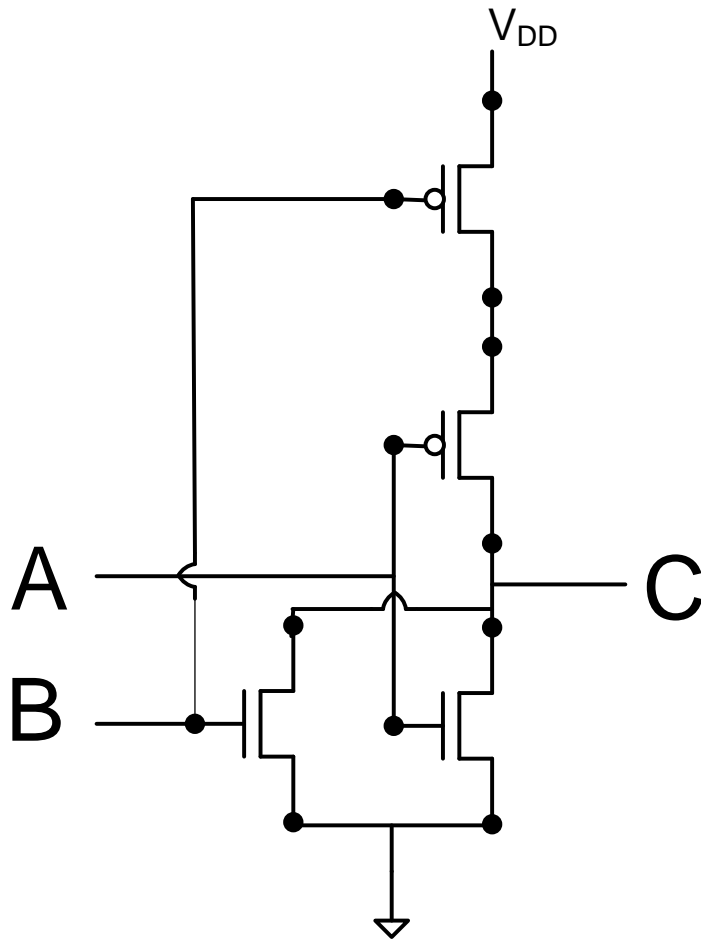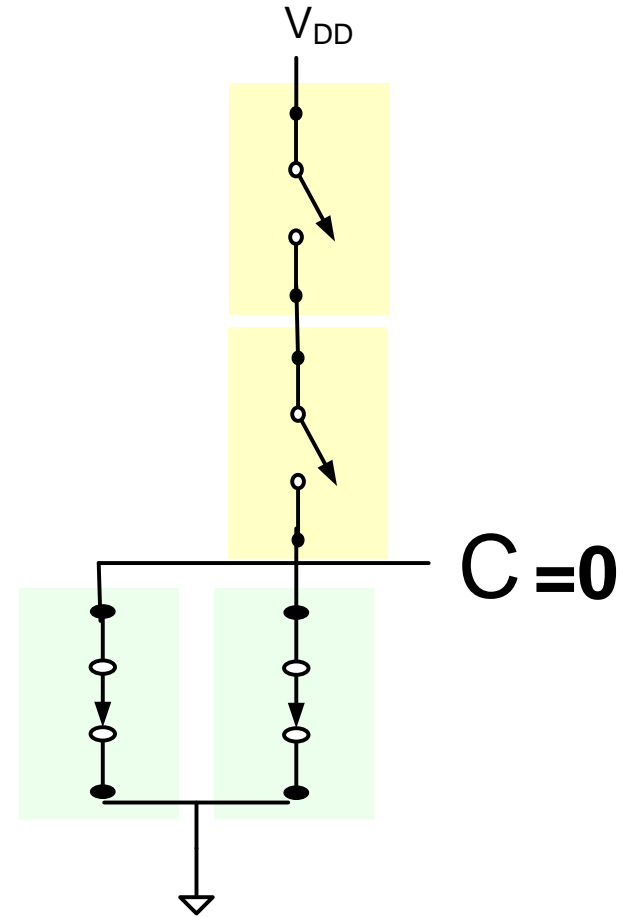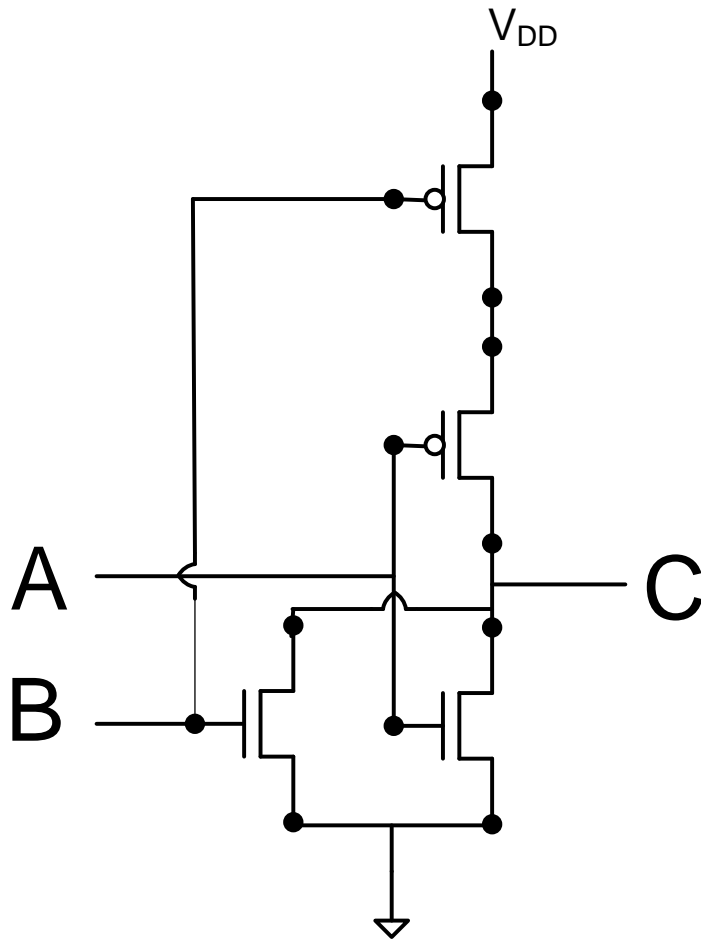
Logic Circuits

NOR Gate

Truth Table

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

Logic Circuits

V$_{DD}$

A

B

C
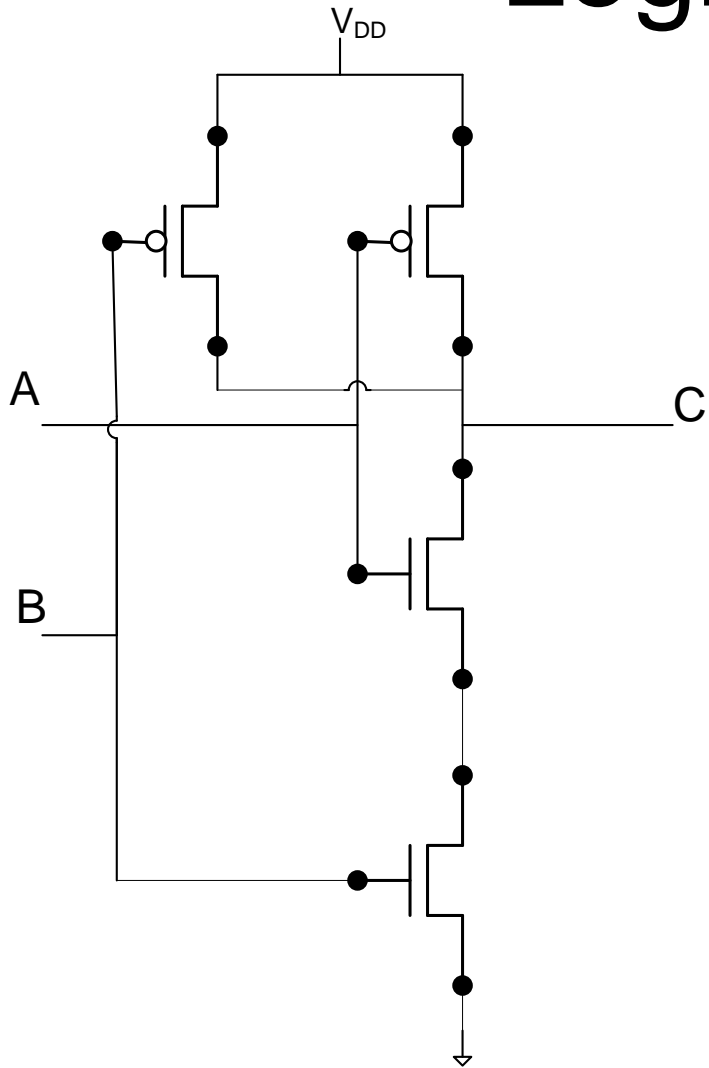
NAND Gate

Truth Table

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

Logic Circuits
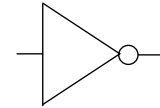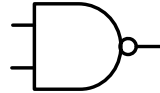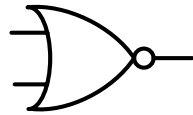
Approach can be extended to arbitrary number of inputs

n-input NOR gate
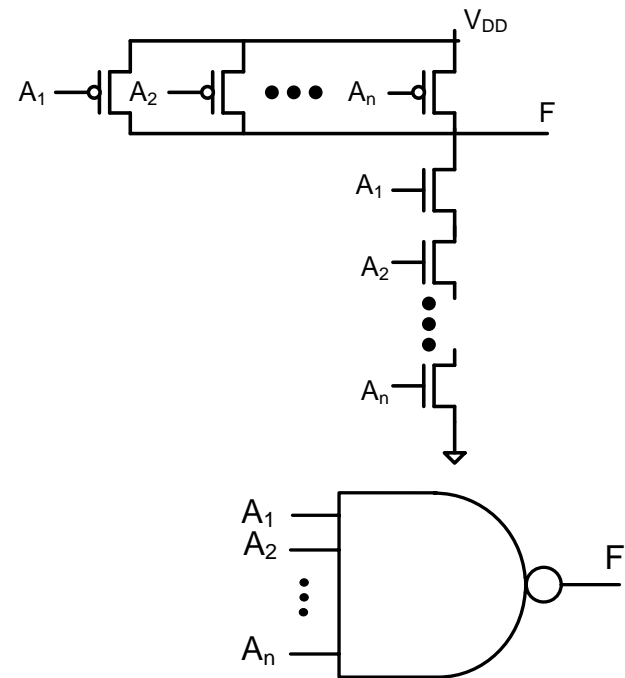
n-input NAND gate

Complete Logic Family
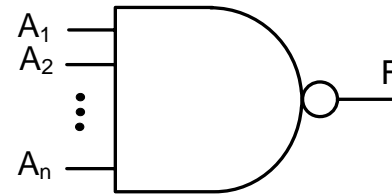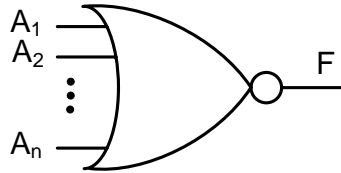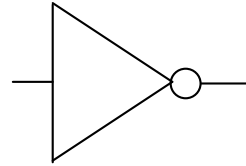
Family of n-input NOR gates forms a complete logic family

Family of n-input NAND gates forms a complete logic family

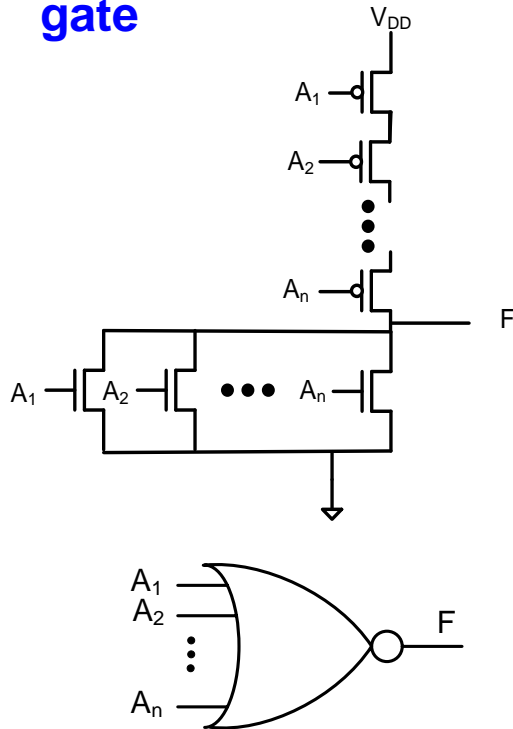**Having both NAND and NOR gates available is a luxury**

Can now implement any combinational logic function !!

If add one flip flop, can implement any Boolean system !!

Flip flops easy to design but will discuss sequential logic systems later

Other logic circuits

- Other methods for designing logic circuits exist

- Insight will be provided on how other logic circuits evolve

- Several different types of logic circuits are often used simultaneously in any circuit design

Pull-up and Pull-down Networks
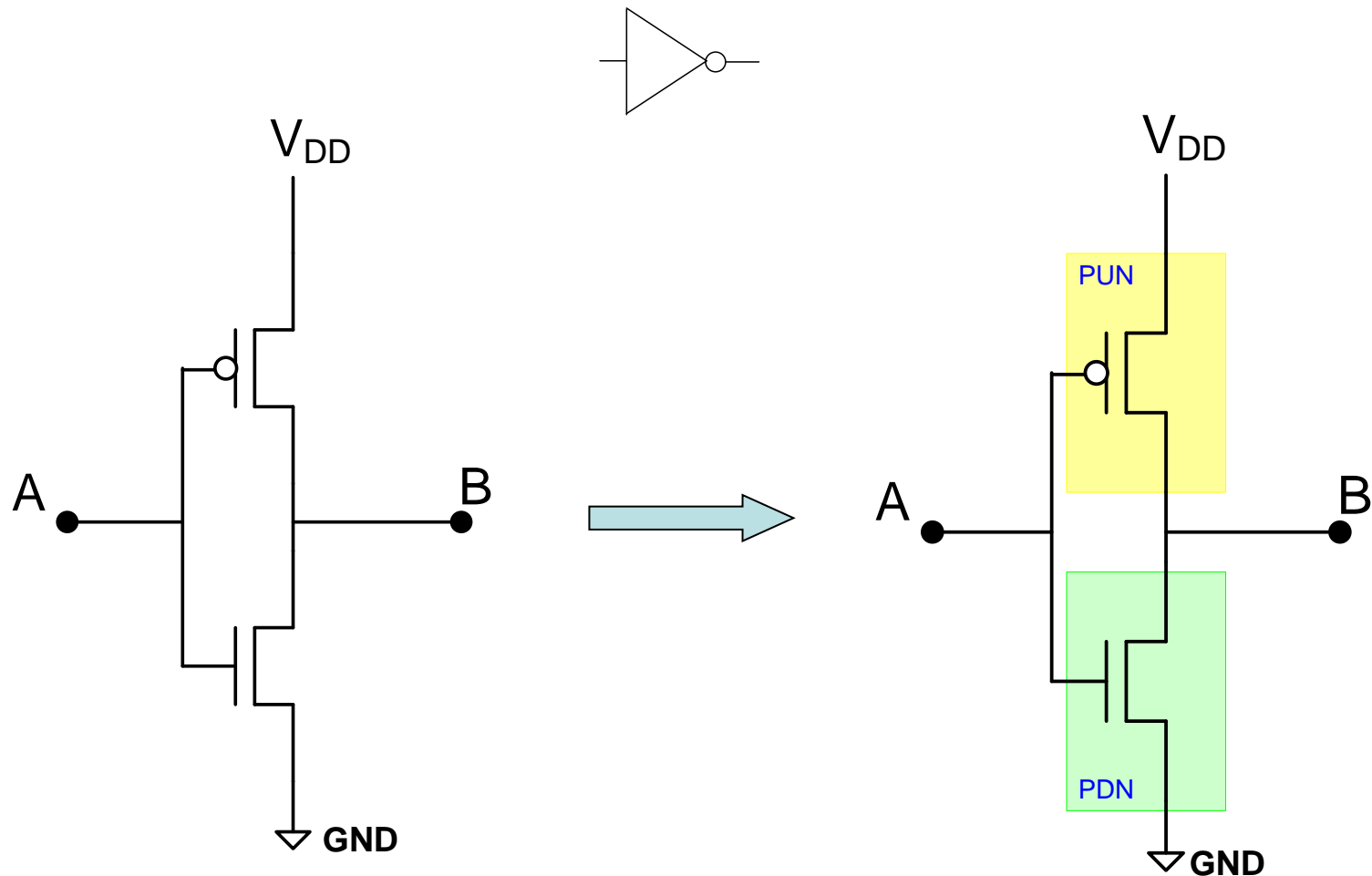
**PU network comprised of p-channel device and "tries" to pull B to VDD when conducting
PD network comprised of n-channel device and "tries to pull B to GND when conducting
One and only one of these networks is conducting at the same time (to avoid contention)**

Pull-up and Pull-down Networks
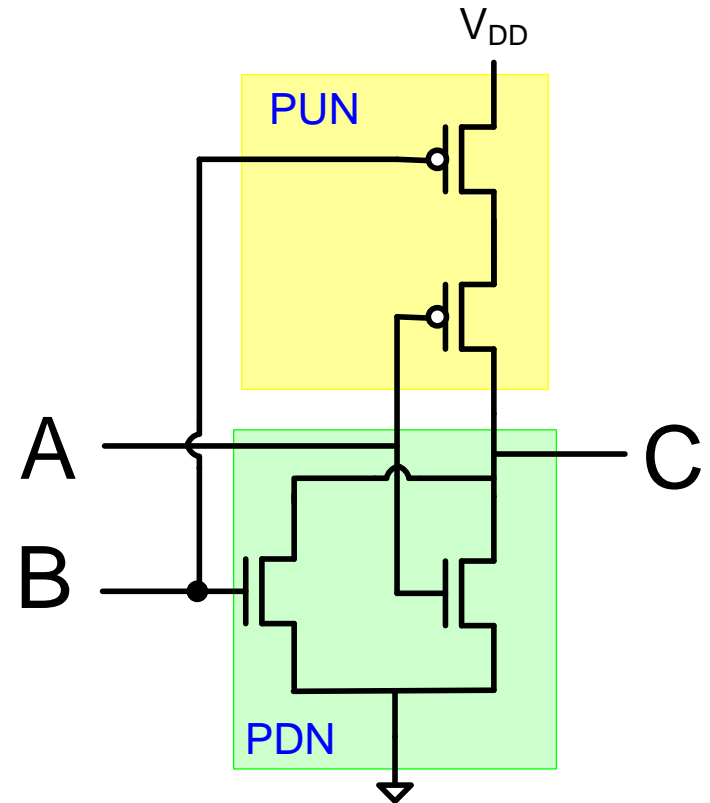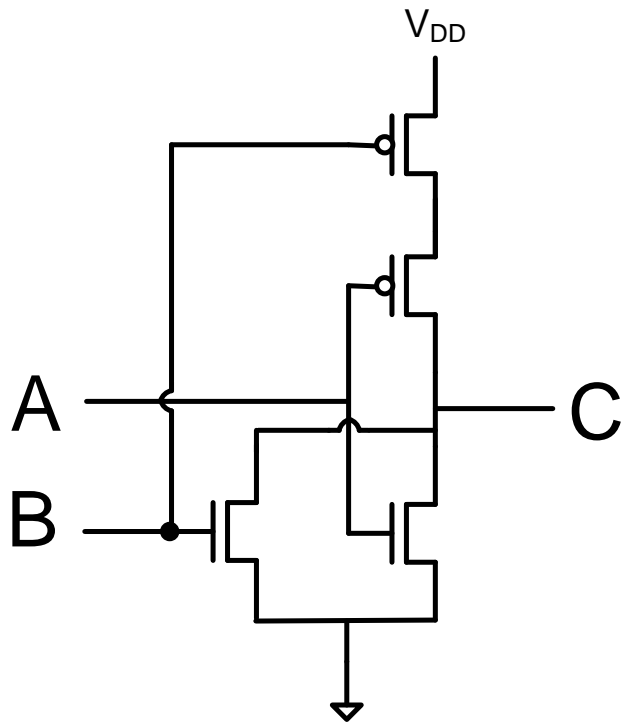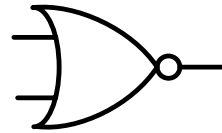
PU network comprised of p-channel devices
PD network comprised of n-channel devices
One and only one of these networks is conducting at the same time

Pull-up and Pull-down Networks

PU network comprised of p-channel devices
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Pull-up and Pull-down Networks
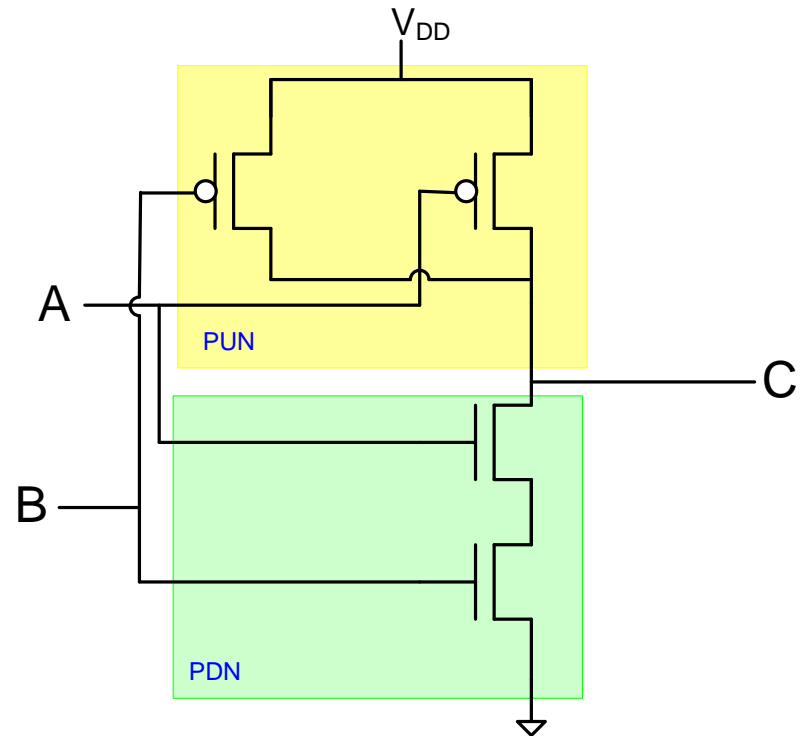
In these circuits, the PUN and PDN have the 3 interesting characteristics
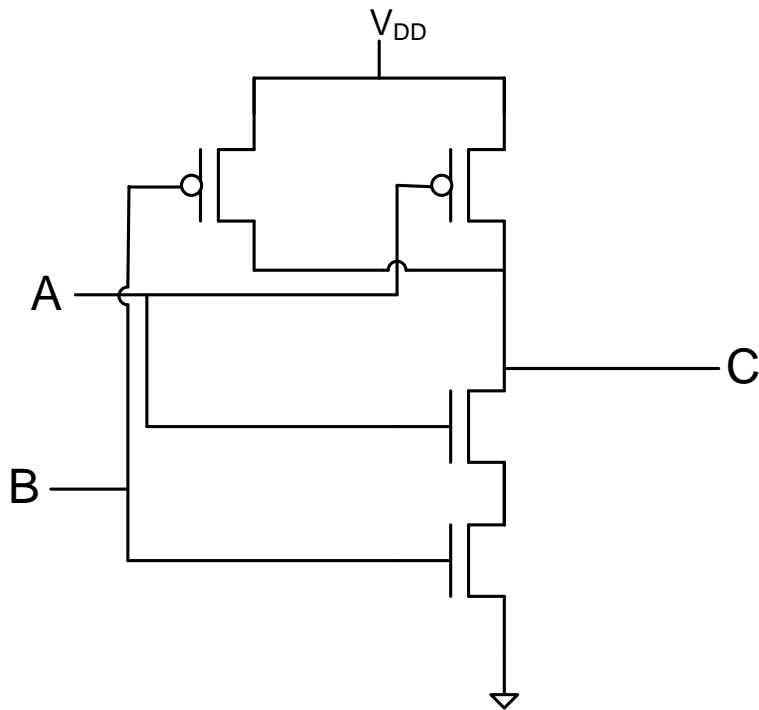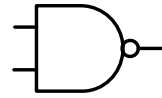
1. **PU network comprised of p-channel devices**
2. **PD network comprised of n-channel devices**
3. **One and only one of these networks is conducting at the same time**

V_{DD}

PUN

X — n — Y

PDN
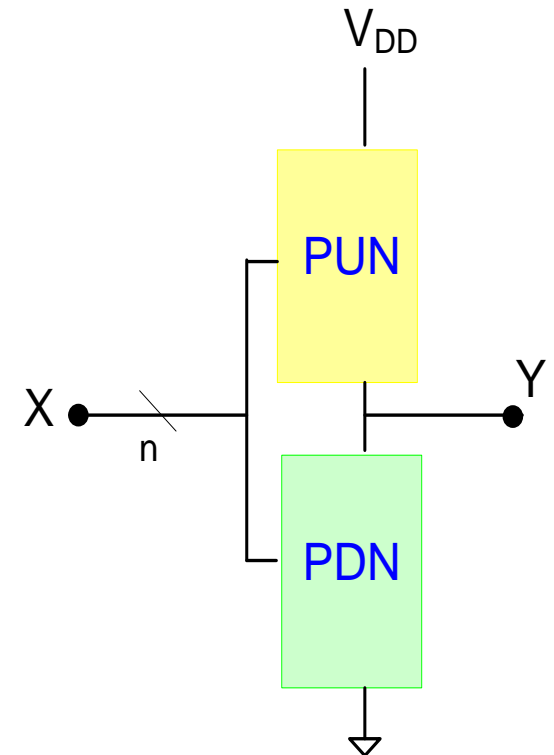
What are V_H and V_L?
What is the power dissipation?
How fast are these logic circuits?

What are V_H and V_L?
What is the power dissipation?
How fast are these logic circuits?

Consider the inverter

Use switch-level model for MOS devices

What are V_H and V_L?
What is the power dissipation?
How fast are these logic circuits?

Consider the inverter

Use switch-level model for MOS devices
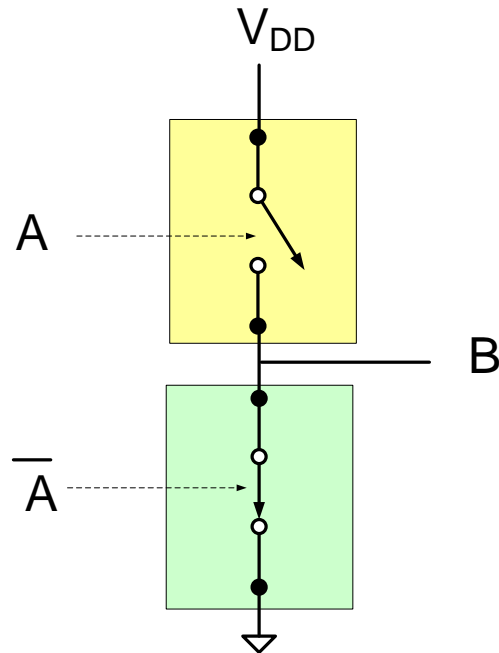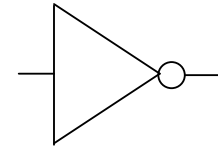
$V_H = V_{DD}$

$V_L = 0$

$I_D = 0$ thus $P_H = P_L = 0$

$t_{HL} = t_{LH} = 0$

(too good to be true?)

Pull-up and Pull-down Networks
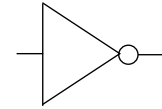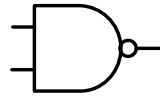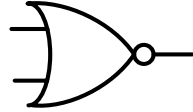
For these circuits, the PUN and PDN have 3 interesting characteristics

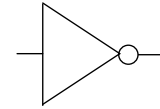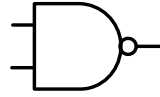**Three key <u>characteristics</u> of these Static CMOS Gates**

1. **PU network comprised of p-channel devices**
2. **PD network comprised of n-channel devices**
3. **One and only one of these networks is conducting at the same time**

Three key <u>properties</u> of these Static CMOS Gates

1. **What are V_H and V_L?**
   $$V_H = V_{DD}, \ V_L = 0 \text{ (too good to be true?)}$$
2. **What is the power dissipation?**
   $$P_H = P_L = 0 \text{ (too good to be true?)}$$
3. **How fast are these logic circuits?**
   $$t_{HL} = t_{LH} = 0 \text{ (too good to be true?)}$$

V_{DD}

PUN

Y

X

n

PDN
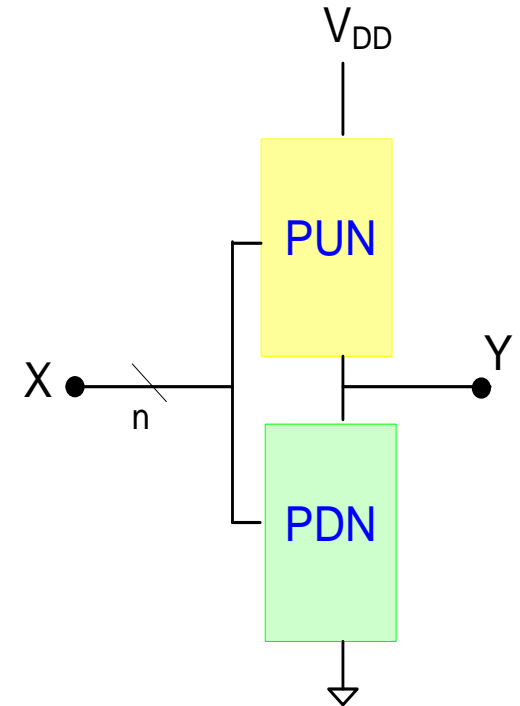
These 3 <u>properties</u> are inherent in all Boolean circuits that have these 3 <u>characteristics</u> !!!

Pull-up and Pull-down Networks

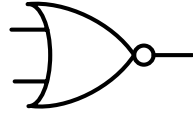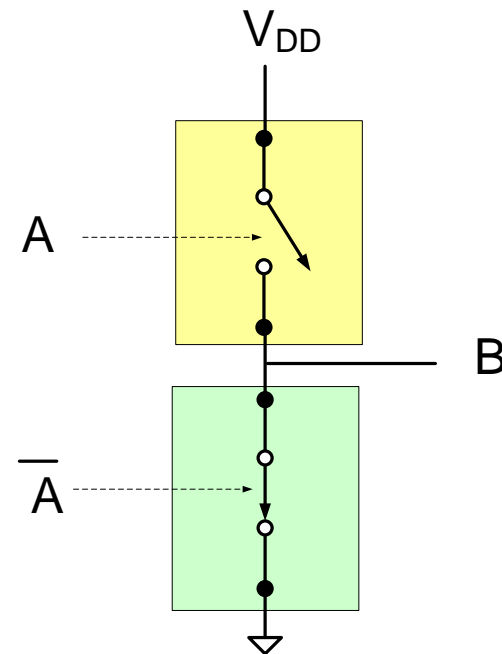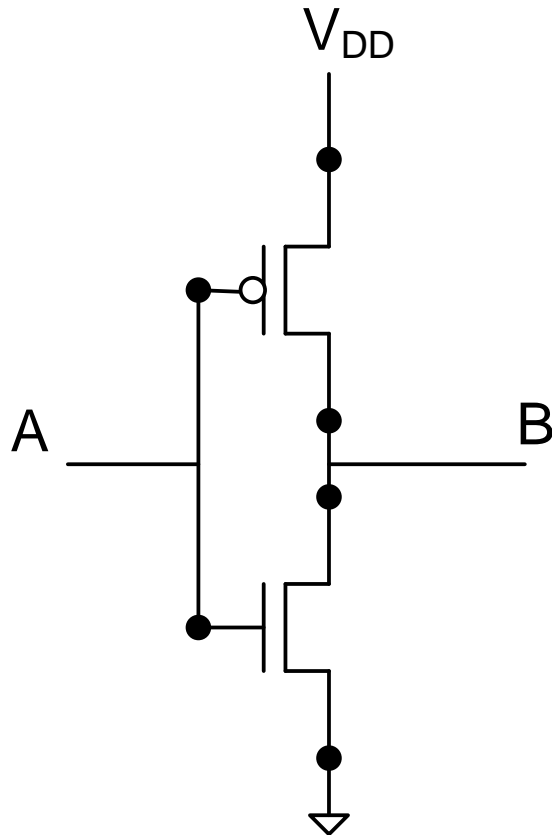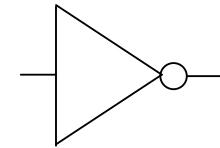**Three key characteristics of Static CMOS Gates**

1. PU network comprised of p-channel devices
2. PD network comprised of n-channel devices
3. One and only one of these networks is conducting at the same time

Three properties of Static CMOS Gates (based upon simple switch-level model)

1. $V_H=V_{DD}$, $V_L=0$ (too good to be true?)
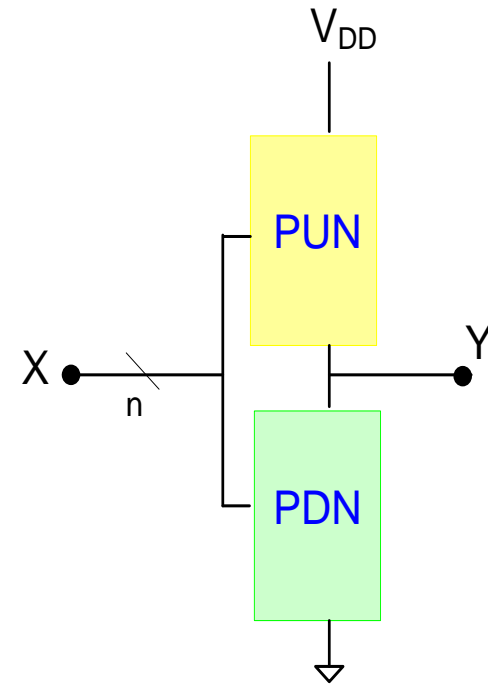
2. $P_H=P_L=0$ (too good to be true?)

3. $t_{HL}=t_{LH}=0$ (too good to be true?)

V_{DD}

PUN

X   n   Y

PDN

These 3 __properties__ are inherent in Boolean circuits with these 3 __characteristics__

Pull-up and Pull-down Networks

Concept can be extended to arbitrary number of inputs
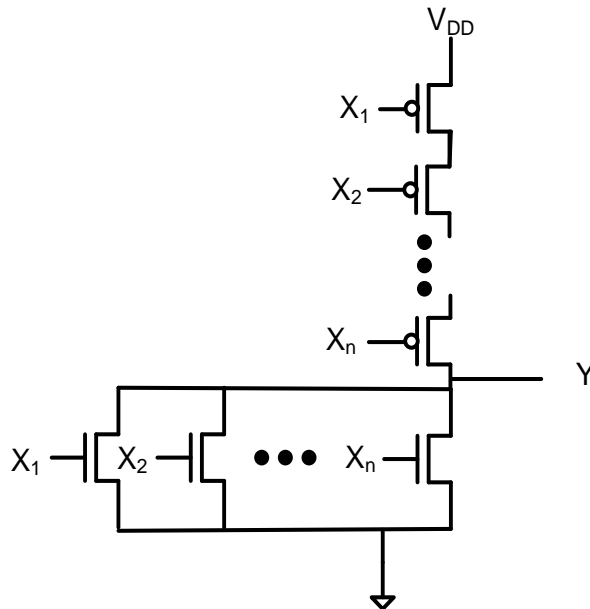
n-input NOR gate

n-input NAND gate

Pull-up and Pull-down Networks
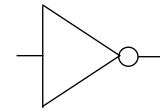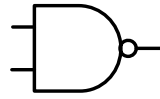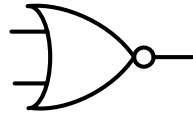
Concept can be extended to arbitrary number of inputs

n-input NOR gate

n-input NAND gate

1. **PU network comprised of p-channel devices**
2. **PD network comprised of n-channel devices**
3. **One and only one of these networks is conducting at the same time**

Pull-up and Pull-down Networks

n-input NOR gate
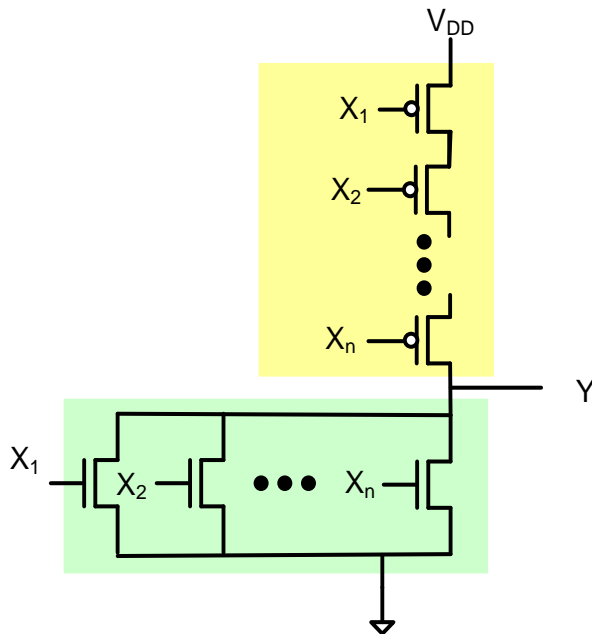
n-input NAND gate
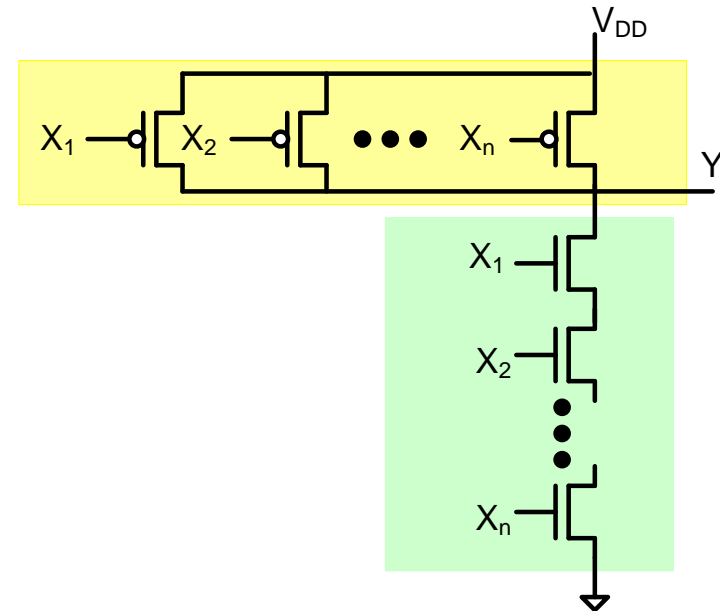
1. PU network comprised of p-channel devices
2. PD network comprised of n-channel devices
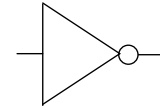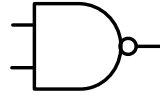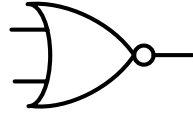3. One and only one of these networks is conducting at the same time

$$V_H = V_{DD}, \quad V_L = 0$$

$$P_H = P_L = 0$$

$$t_{HL} = t_{LH} = 0$$

Nomenclature
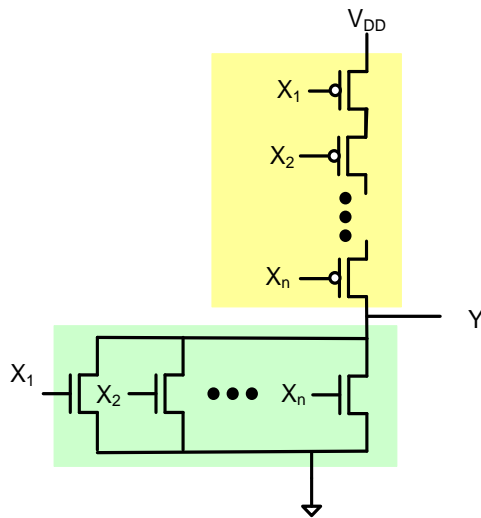
n-input NOR gate
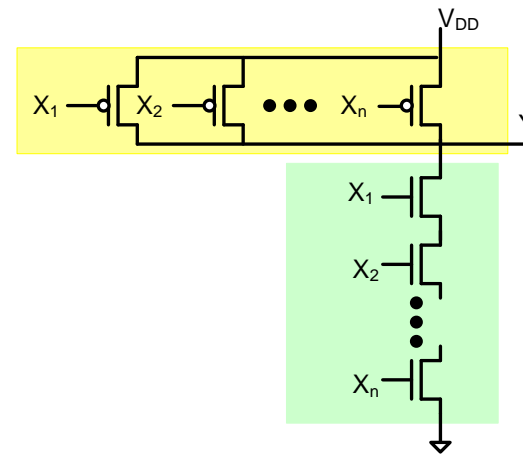
n-input NAND gate

In this class, logic circuits that are implemented by interconnecting multiple-input NAND and NOR gates will be referred to as "Static CMOS Logic"

Since the set of NAND gates is complete, any combinational logic function can be realized with the NAND circuit structures considered thus far

Since the set NOR gates is complete, any combinational logic function can be realized with the NOR circuit structures considered thus far

Many logic functions are realized with "Static CMOS Logic" and this is probably the dominant design style used today!

Example 1:
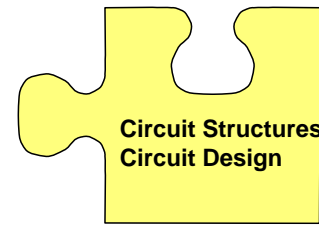
How many transistors are required to realize the function

$$F = \overline{A \bullet \overline{\overline{B}}} + \overline{A} \bullet C$$

in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available.

Example 1:

How many transistors are required to realize the function

$$F = \overline{A \bullet \overline{B} + \overline{A} \bullet C}$$

in a basic CMOS process if static NAND and NOR gates are used?   Assume A, B and C are available.
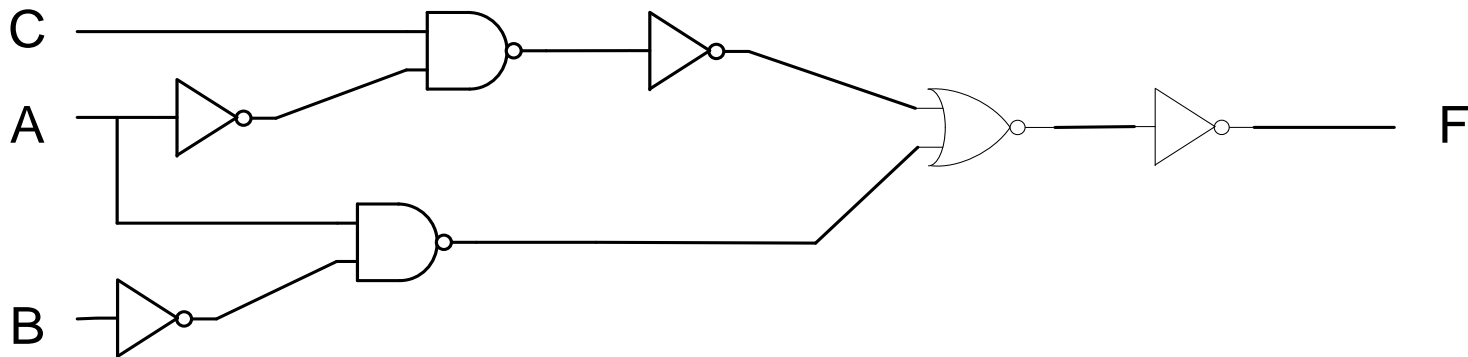
Solution:

20 transistors and 5 levels of logic

Example 1:

How many transistors are required to realize the function

$$F = \overline{A \bullet \overline{B}} + \overline{A} \bullet C$$

in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available.

Solution (alternative):   **From basic Boolean Manipulations**

$$F = \overline{A} + \overline{\overline{B}} + \overline{A} \bullet C = \overline{A} + B + \overline{A} \bullet C$$

$$F = \overline{A} \bullet (1 + C) + B = \overline{A} + B$$
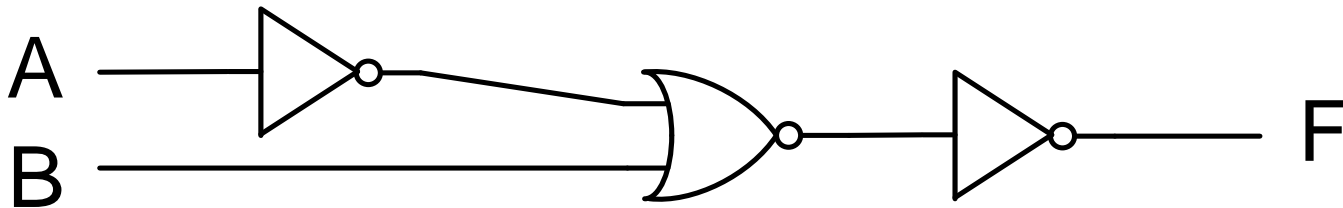
8 transistors and 3 levels of logic

Example 1:

How many transistors are required to realize the function

$$F = \overline{A \bullet \overline{B}} + \overline{A} \bullet C$$

in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available.

Solution (alternative):   **From basic Boolean Manipulations**

$$F = \overline{A} \bullet (1 + C) + B = \overline{A} + B$$

$$F = \overline{\overline{\overline{A} + B}} = \overline{A \bullet \overline{B}}$$
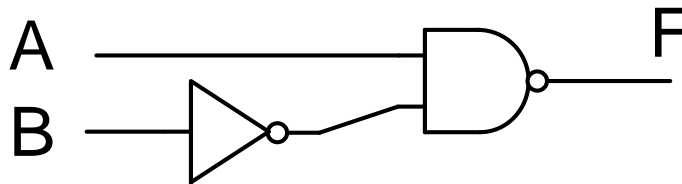
6 transistors and 2 levels of logic

Example 2: XOR Function

A ⟩⟩⊃ Y
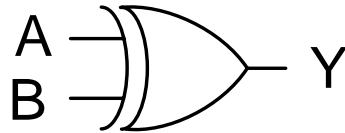
$$Y = A \oplus B$$

A widely-used 2-input Gate

Static CMOS implementation

$$Y = A\bar{B} + \bar{A}B$$
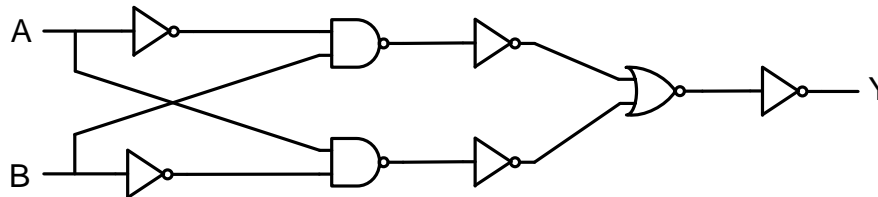
22 transistors   5 levels of logic

Delays unacceptable (will show later) and device count is too large !

Example 3:

$$Y = \overline{(A \bullet B) + (C \bullet D)}$$

Standard Static CMOS Implementation
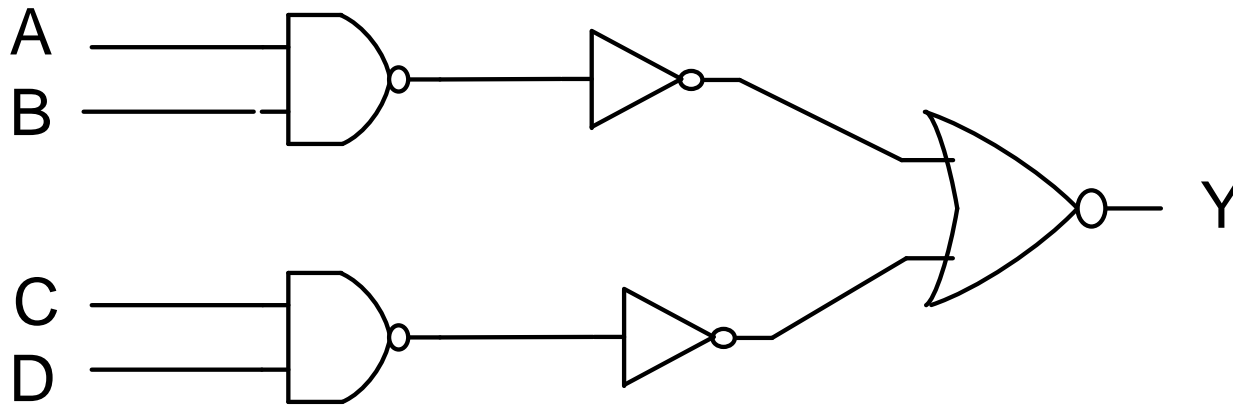
3 levels of Logic

16 Transistors if Basic CMOS Gates are Used

Can the same Boolean functionality be obtained with less transistors?

Complex Logic Gates

Some circuits other than multiple-input NAND and NOR gates can also have the three key characteristics

Three key characteristics of low static power CMOS logic
1. PU network comprised of p-channel devices
2. PD network comprised of n-channel devices
3. One and only one of these networks is conducting at the same time

Three properties of circuits with these 3 characteristics

1. $V_H = V_{DD}$, $V_L = 0$ (too good to be true?)

2. $P_H = P_L = 0$ (too good to be true?)

3. $t_{HL} = t_{LH} = 0$ (too good to be true?)
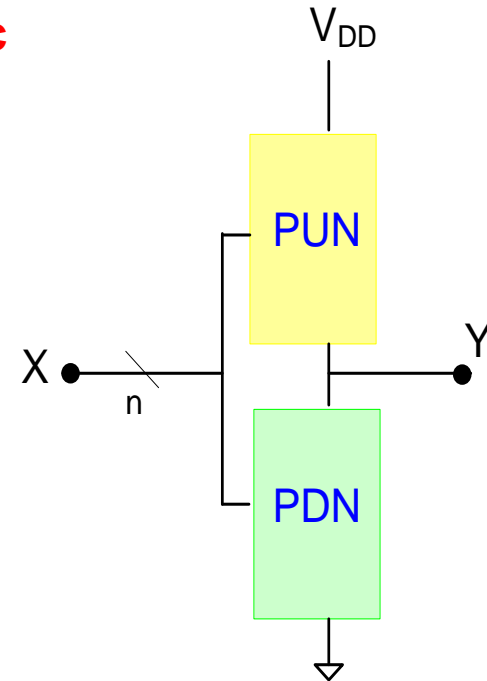
These 3 properties are inherent in Boolean circuits with these 3 characteristics
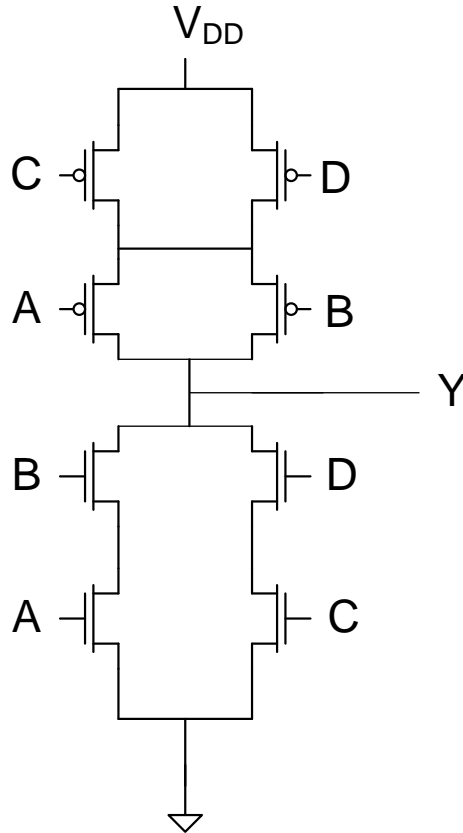
Observe:
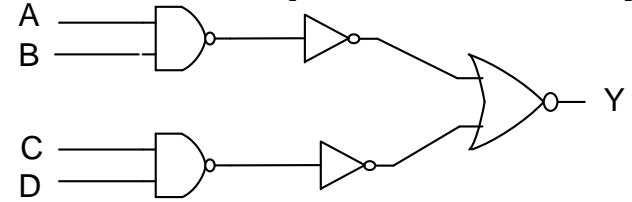
$$Y = \overline{(A \bullet B) + (C \bullet D)}$$

3 levels of Logic, 16 Transistors if Basic CMOS Gates are Used

$$Y = \overline{(A \bullet B) + (C \bullet D)}$$

1 level of logic and 8 transistors in this example

Significant reduction in transistor count and levels of logic for realizing same Boolean function

Termed a "Complex Logic Gate" implementation

Some authors term this a "compound gate"

Complex Logic Gates
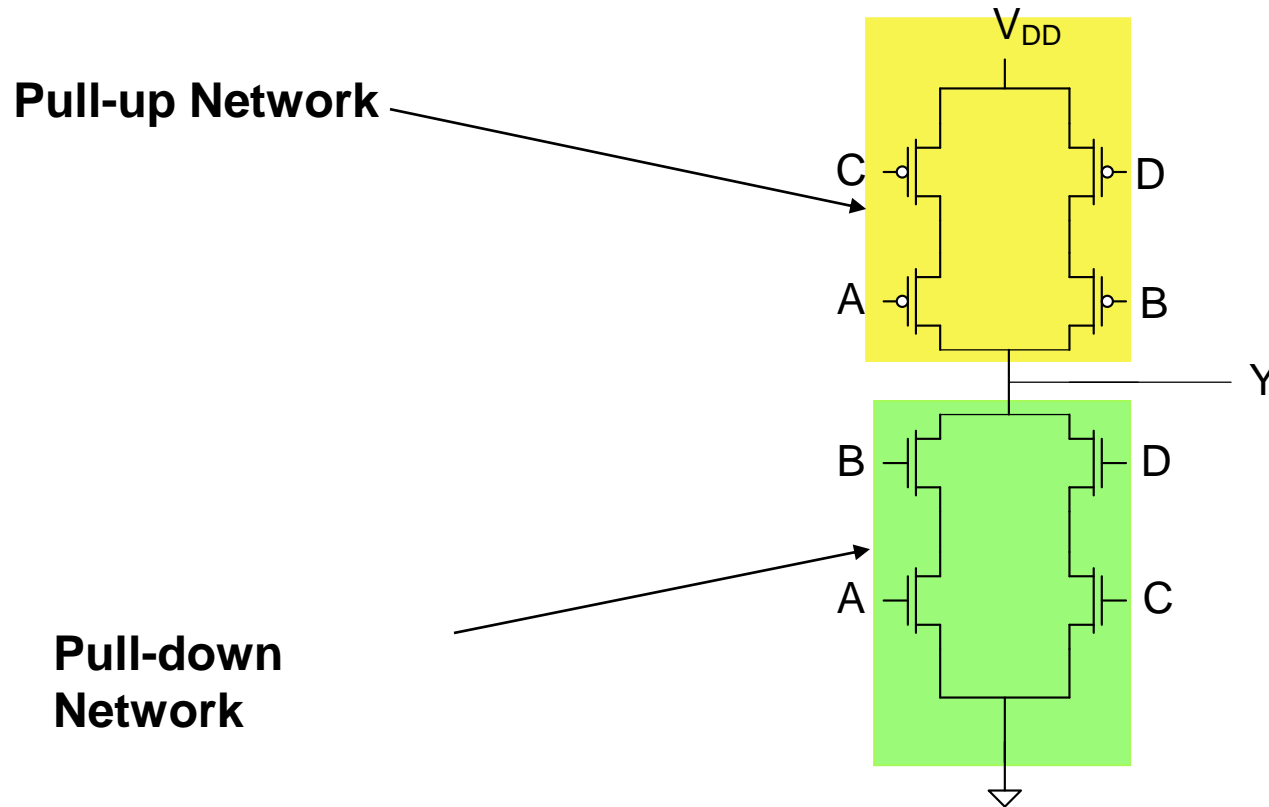
$$Y = \overline{(A \bullet B) + (C \bullet D)}$$

Complex Gates

1. **PU network comprised of p-channel devices**
2. **PD network comprised of n-channel devices**
3. **One and only one of these networks is conducting at the same time**
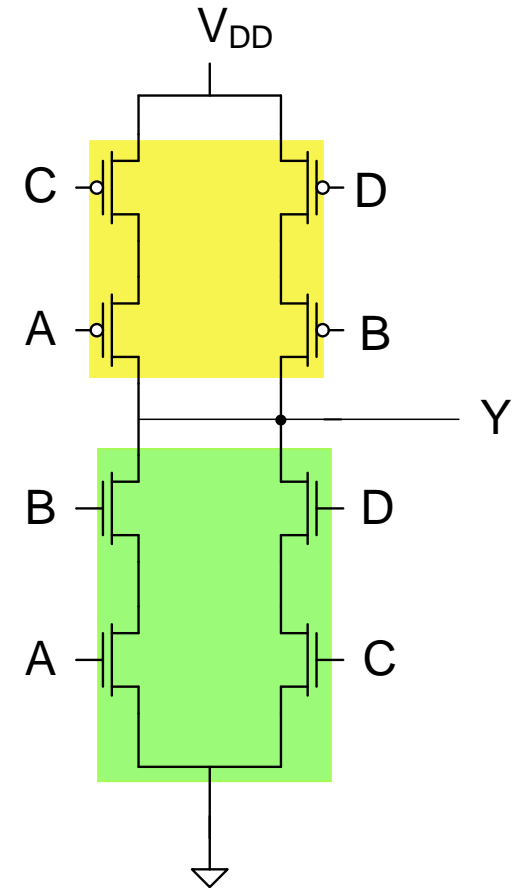
Complex Gates

Nomenclature:
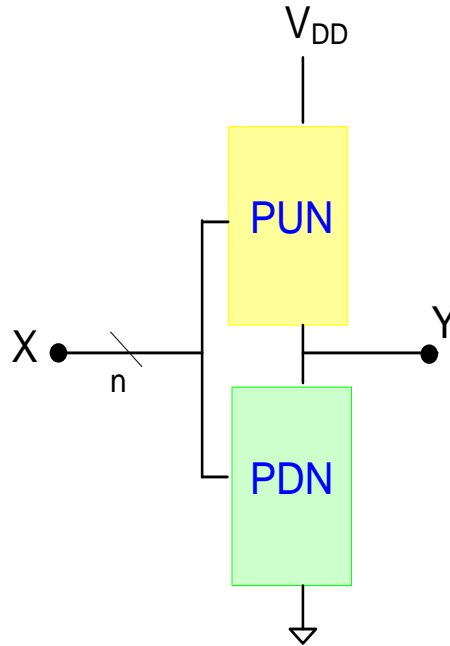
When the logic gate shown is not a multiple-input NAND or NOR gate but has Characteristics 1, 2, and 3 above, the gate will be referred to as a Complex Logic Gate

Complex Logic Gates also implement static logic functions and some authors would refer to this as Static CMOS Logic as well but we will make the distinction and refer to this as "Complex Logic Gates"

Complex Gates
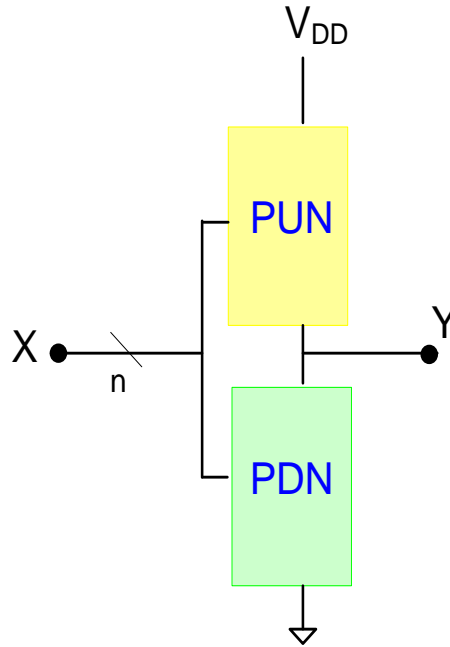
Complex Gate Design Strategy:

1. Implement $\overline{Y}$ in the PDN

2. Implement Y in the PUN (must complement the input variables since p-channel devices are used)

   (Y and $\overline{Y}$ often expressed in either SOP or POS form)

XOR in Complex Logic Gates
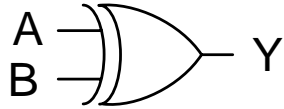
A ——⟩⟩ — Y $Y = A \oplus B$
B ——

Will express $\overline{Y}$ and Y in standard SOP or POS form

XOR in Complex Logic Gates

A ⟩⟩ Y
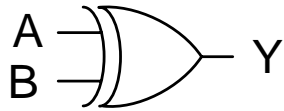
$$Y = A \oplus B$$

$$Y = A\overline{B} + \overline{A}B$$

$$\overline{Y} = \overline{\left(A\overline{B} + \overline{A}B \right)}$$

$$\overline{Y} = \overline{A\overline{B}} \bullet \overline{\overline{A}B}$$

$$\overline{Y} = (\overline{A} + B) \bullet (A + \overline{B})$$

XOR in Complex Logic Gates
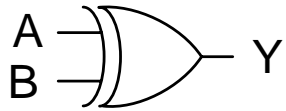
$$Y=A\overline{B} + \overline{A}B$$
$$\overline{Y}=(\overline{A}+B)\bullet(A+\overline{B})$$

PDN
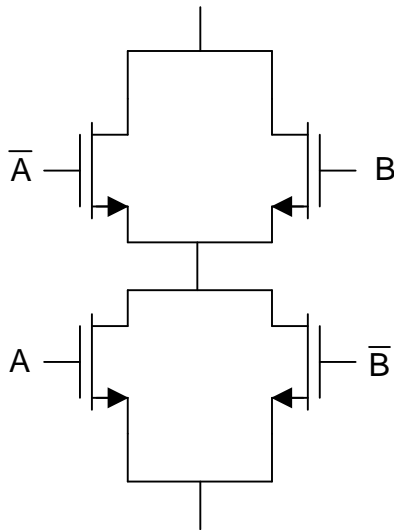
PUN
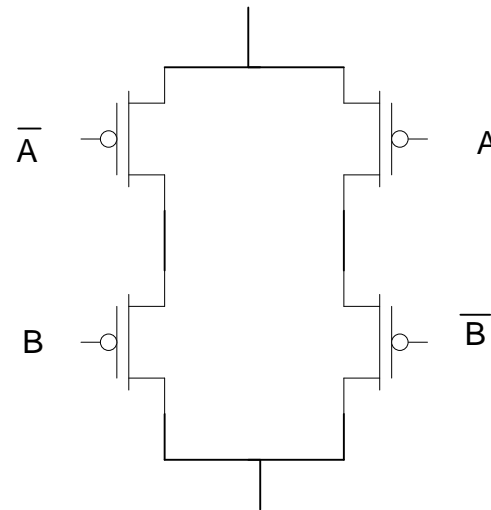
XOR in Complex Logic Gates
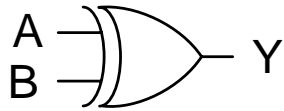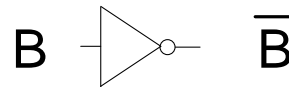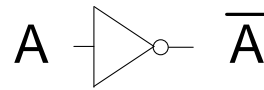
$$Y = A\overline{B} + \overline{A}B$$

$$\overline{Y} = (\overline{A} + B) \cdot (A + \overline{B})$$

12 transistors and 2 levels of logic

Notice a significant reduction in the number of transistors required
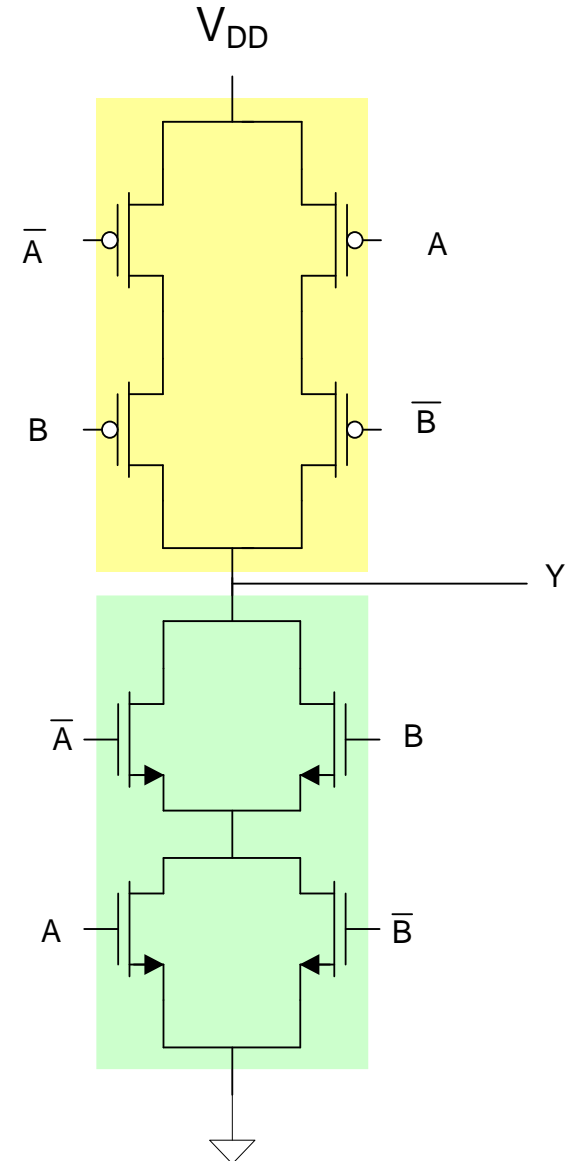
XOR in Complex Logic Gates
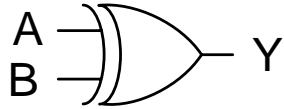
$$Y=A\overline{B} + \overline{A}B$$

$$\overline{Y}=(\overline{A}+B)\cdot(A+\overline{B})$$

Multiple PU and PD networks can be used

$$\overline{Y}=(\overline{A}+B)\cdot(A+\overline{B})$$

$$=(\overline{A}\cdot(A+\overline{B}))+(B\cdot(A+\overline{B}))$$

$$=(\overline{A}\cdot\overline{B})+(A\cdot B)$$
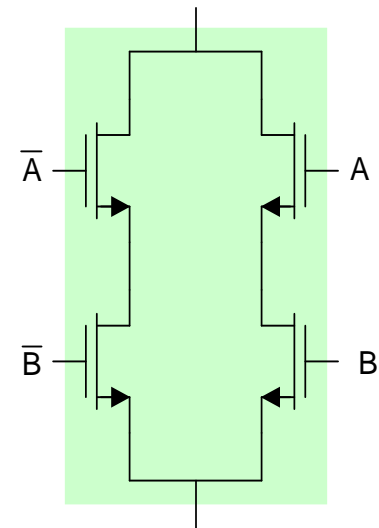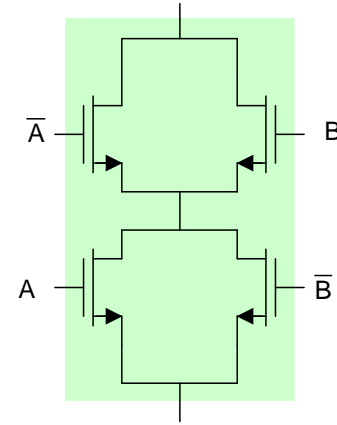
Complex Logic Gate Summary:

V_{DD}

PUN

X •———/———| |———• Y
    n

PDN
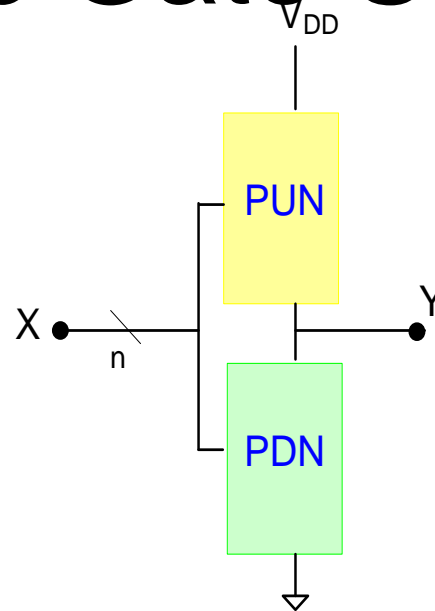
If PUN and PDN satisfy the characteristics:

1. PU network comprised of p-channel device
2. PD network comprised of n-channel device
3. One and only one of these networks is conducting at the same time

Properties of PU/PD logic of this type (with simple switch-level model):

Rail to rail logic swings
Zero static power dissipation in both Y=1 and Y=0 states
Arbitrarily fast (too good to be true? will consider again with better model)

$\Rightarrow$ Pass Transistor Logic

- Improved Switch-Level Model
- Propagation Delay
- Stick Diagrams
- Technology Files

Consider $\quad \mathbf{Y} = \mathbf{A} \bullet \mathbf{B}$

Standard CMOS Implementation
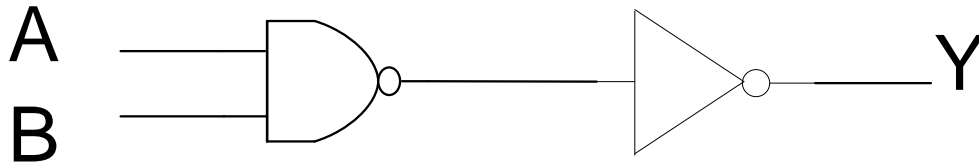
2 levels of Logic

6 Transistors if Basic CMOS Gates are Used

Basic noninverting functions generally require more complexity if basic CMOS gates are used for implementation

Pass Transistor Logic
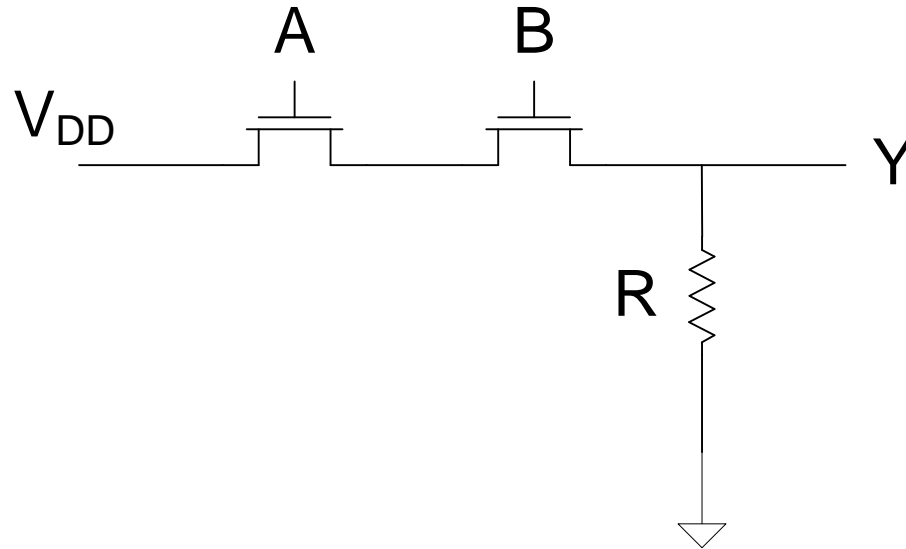
$$Y = A \bullet B$$

Requires only 2 transistors rather than 6 for a standard CMOS gate (and a resistor).

Pass Transistor Logic
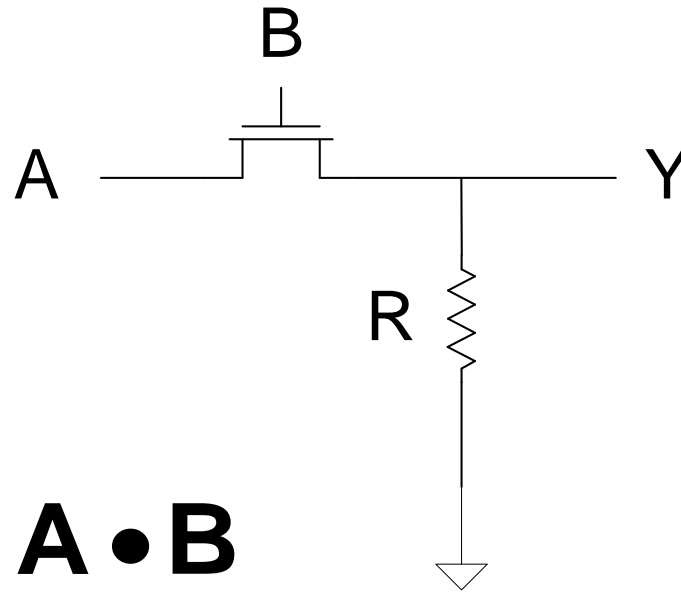
$$Y = A \cdot B$$

Even simpler pass transistor logic implementations are possible

Requires only 1 transistor (and a resistor).

Will see later that the area of a single practical resistor for this circuit may be comparable to that needed for hundreds or even thousands of transistors

Pass Transistor Logic

$$Y = A \bullet B$$
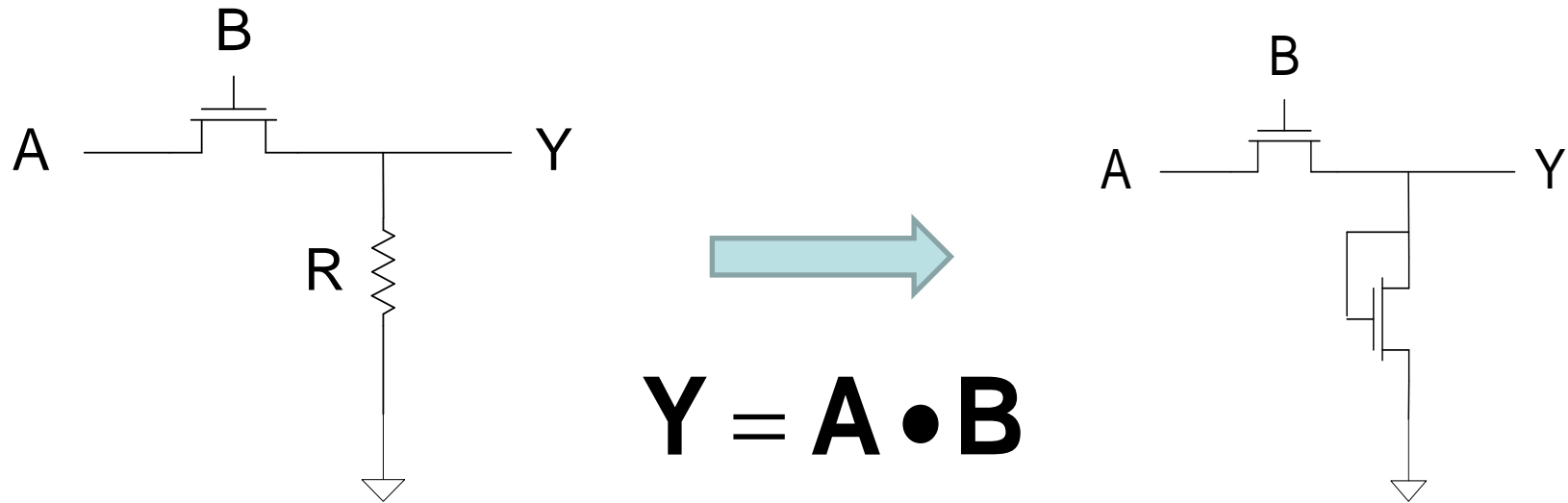
- **May be able to replace resistor with transistor (one of several ways shown)**

- **But high logic level can not be determined with existing device model (or even low logic level for circuit on right)**

- **Power dissipation can not be determined with existing device model for circuit on right**

Better device model is needed (Power? Signal Swing? Speed?)

Pass Transistor Logic
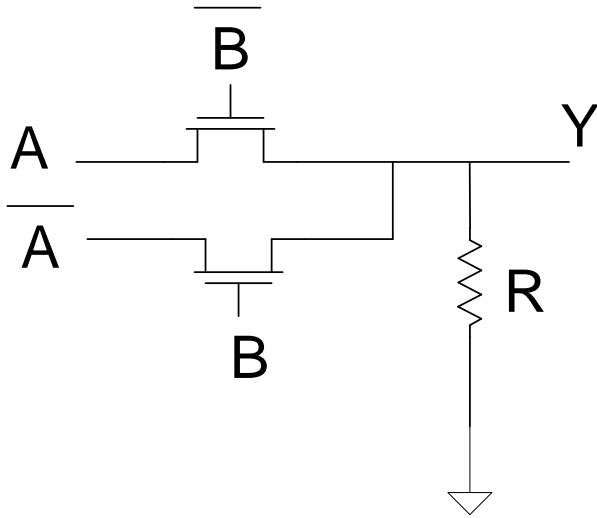
$$Y = A \oplus B$$

6 transistors, 1 resistor, two levels of logic

(the 4 transistors in the two inverters are not shown)

Pass Transistor Logic

$$Y = A \oplus B$$

$$Y = A \oplus B$$

2 transistors, 1 resistor, one level of logic

Pass Transistor Logic
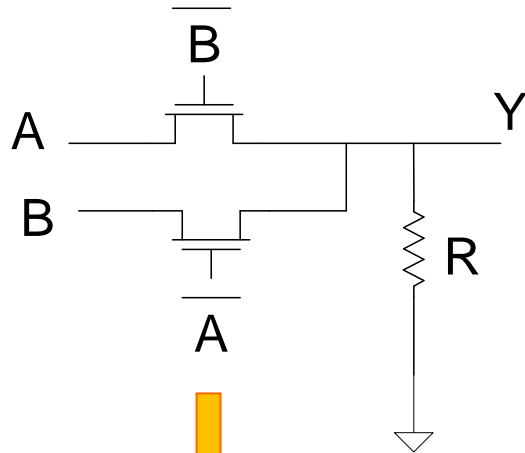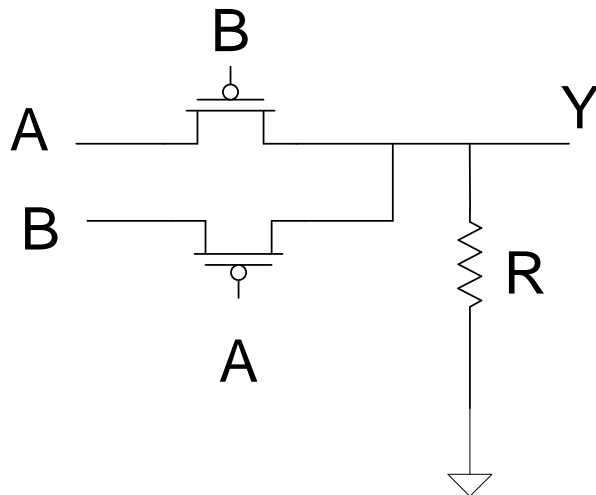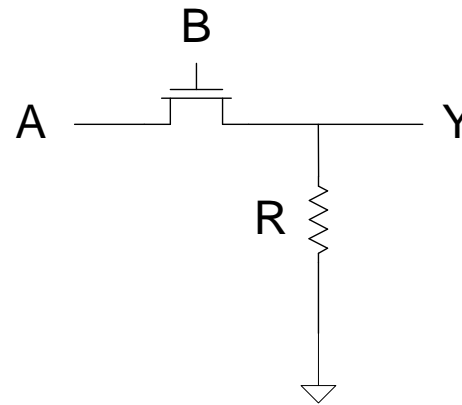

$$Y = A \bullet B$$

Requires only 1 transistor (and a resistor)

- -

- **Pass transistor logic can offer significant reductions in complexity for some functions (particularly noninverting)**
- **Resistor may require more area than several hundred or even several thousand transistors**
- **Signal levels may not go to V_{DD} or to 0V**
- **Static power dissipation may not be zero**
- **Signals may degrade unacceptably if multiple gates are cascaded**
- **"resistor" often implemented with a transistor to reduce area but signal swing and power dissipation problems still persist**
- **Pass transistor logic is widely used**

Logic Design Styles

- Several different logic design styles are often used throughout a given design (3 considered thus far)
  - Static CMOS
  - Complex Logic Gates
  - Pass Transistor Logic
- The designer has complete control over what is placed on silicon and governed only by cost and performance
- New logic design strategies have been proposed recently and others will likely emerge in the future
- The digital designer needs to be familiar with the benefits and limitations of varying logic styles to come up with a good solution for given system requirements

Stay Safe and Stay Healthy !

End of Lecture 6